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REV: X00

PWB: XXXXX

DATE: 1450-06

ZZZ1



PCB ZVR LA-J521P REV0 M/B NVIDIA N18E S

DAB0005V000

PCB@

Dell/Compal Confidential

Schematic Document

(Viper Comet Lake H with nVIDIA N18E)

DVT1

2019-09-24

Rev: 0.2 (X01)

BOM Structure

- PCB@ : PCB PN
- @ : Nopop Component
- EMI@,ESD@,RF@ : EMI/ESD/RF part
- CONN@ : Connector Component
- @EMI@,@ESD@,@RF@ : EMI, ESD and RF Un-POP Component

Board ID Table for AD channel

Vcc 3.3V +/- 1%					
Ra 100K +/- 1%					
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	1.2M +/- 1%	3.020V	3.046V	3.067V	0xF1 - 0xFF

PCIE CLK table

PCIE CLK	PCB Revision
0	GPU
1	SSD2
2	SSD3/WWAN
3	TBT
4	LAN
5	WLAN
6	caldera
7	SSD1

Board ID table

NV			AMD	PCB Revision
N18P	N18E			
	2Stage	1Stage		
0	4	8	12	EVT-1
1	5	9	13	DVT-1
2	6	10	14	DVT-2
3	7	11	15	Pilot

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VSIO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VALW	+1.8VALW power rail for PCH	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

PCH-H CM246

HSIO	USB3.1	PCIe	SATA3	Function	
0	1				
1	2			Card reader	
2	3			Caldera	
3	4			JUSB3 left side	
4	5			JIO right side USB2	
5	6			JIO right side USB1	
6	7	1			
7	8	2			
8	9	3			
9	10	4			
10		5			
11		6			
12		7			
13		8			
14		9		JSSD1 , 2280 SATA/PCIe x4	
15		10			
16		11	0a		
17		12	1a		
18		13	0b	WWAN	JSSD3 PCIe X2
19		14	1b		
20		15	2	LAN	
21		16	3	WLAN	
22		17	4	TBT PCIe X4	
23		18	5		
24		19			
25		20			
26		21		JSSD2 , 2280 PCIe x4	
27		22			
28		23			
29		24			

USB2	Function
1	JUSB3 left side
2	JIO right side USB1
3	Caldera
4	ELC
5	Card reader
6	WWAN
7	Camera
8	JIO right side USB2
9	Tobii
10	Per Key
11	Thunderbolt PD
12	Tron light
13	
14	Bluetooth

Symbol Note :

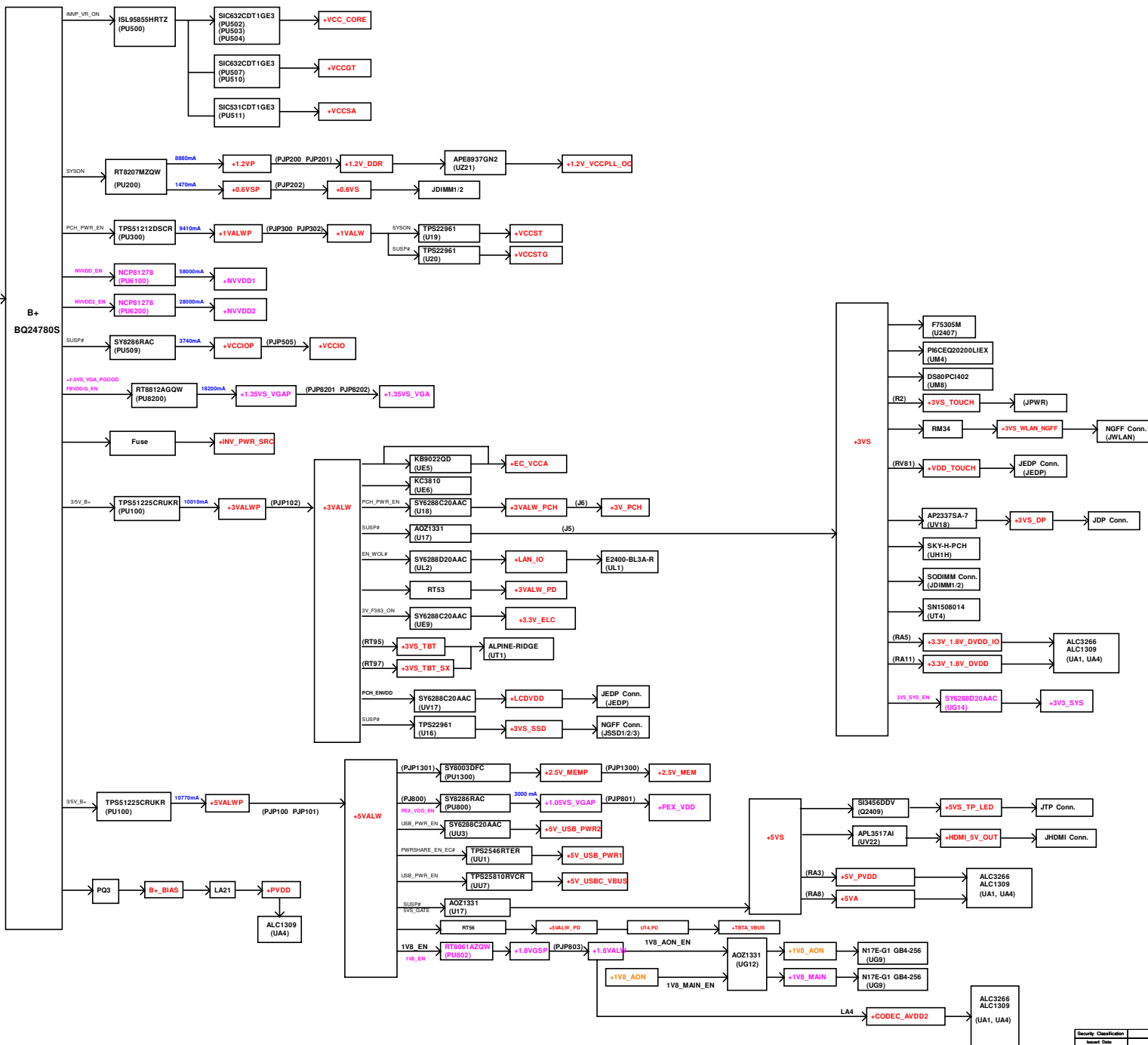
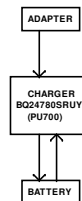


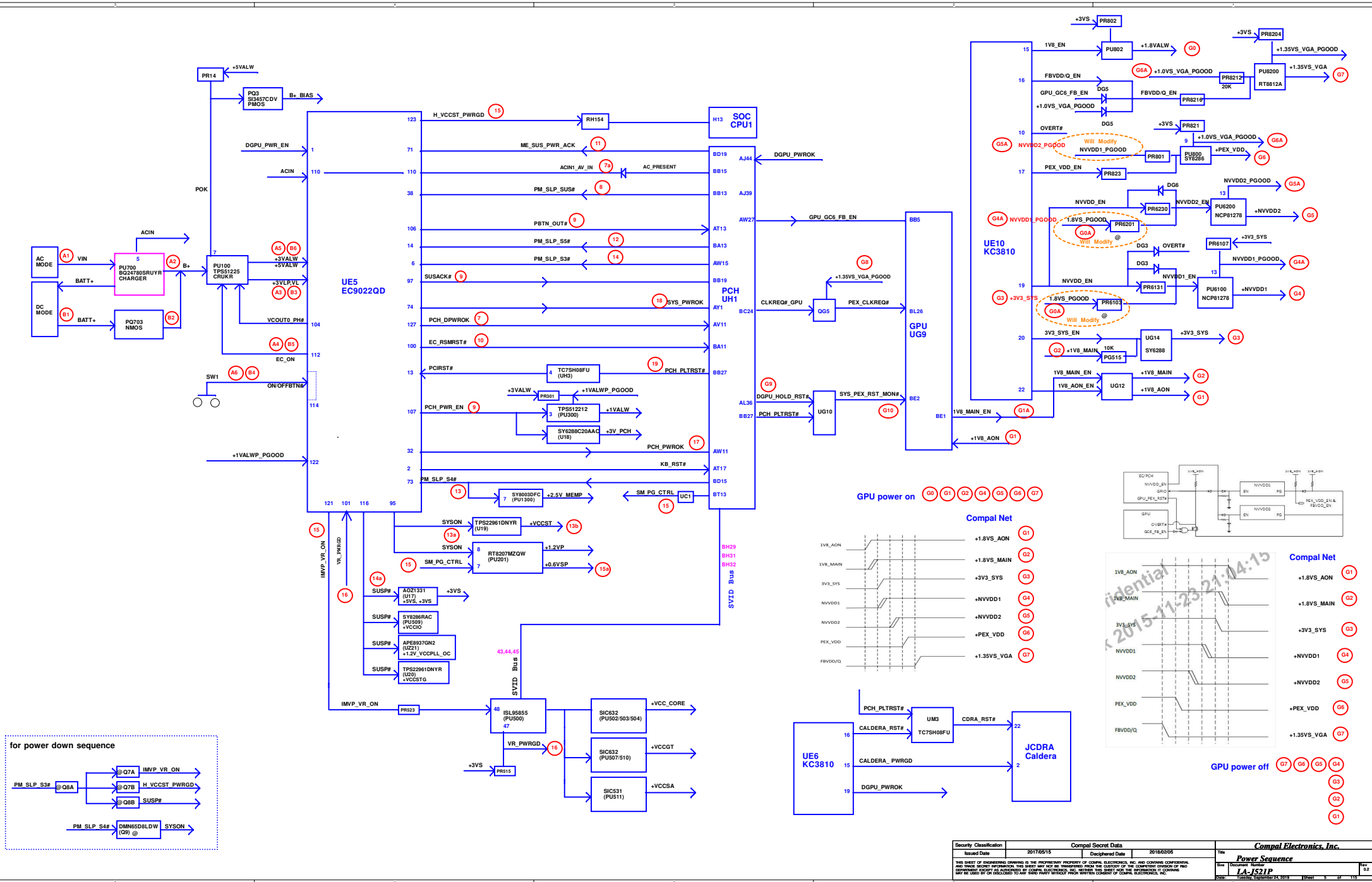
Digital Ground



Analog Ground

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				Date:	Tuesday, September 24, 2019	Sheet 3 of 114







CL8070104399007 QTJ0 R0 2.8G S
SA000003N0L
QTJ0@



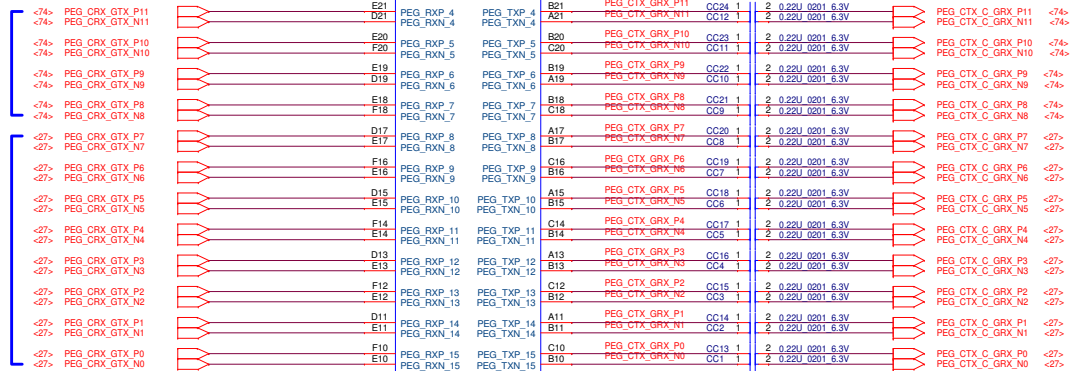
CL8070104398806 QTJ1 R0 2.1G S
SA000003N0L
QTJ1@



S IC A31 CL8070104398908 QTJ2 R0 2.4G S
SA000003N0L
QTJ2@

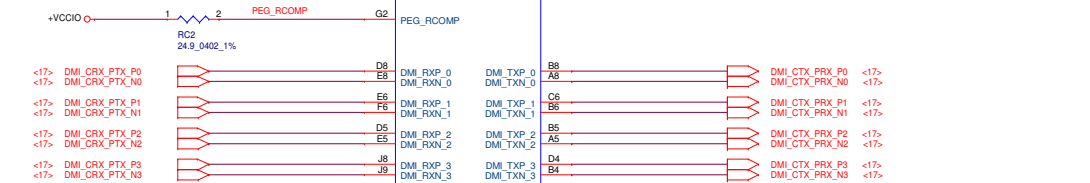
Caldera TX

GPU TX

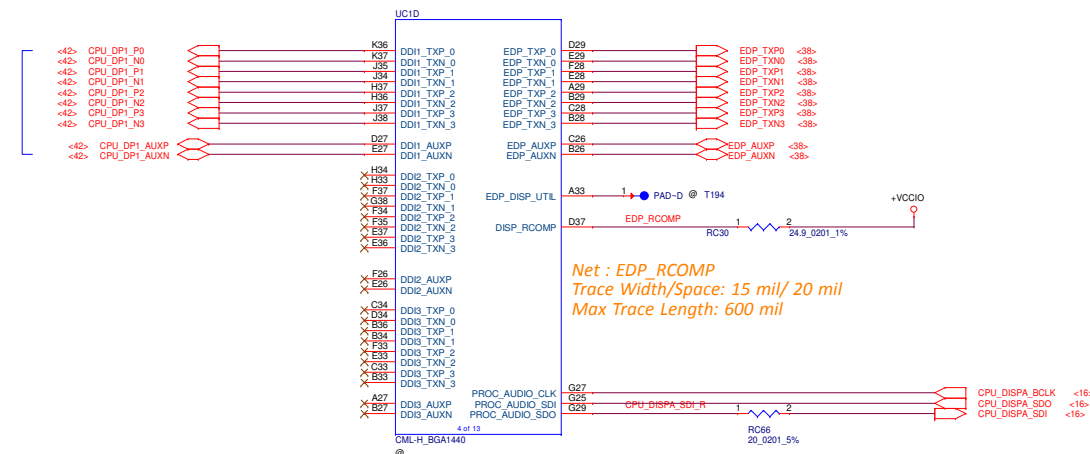


Caldera RX

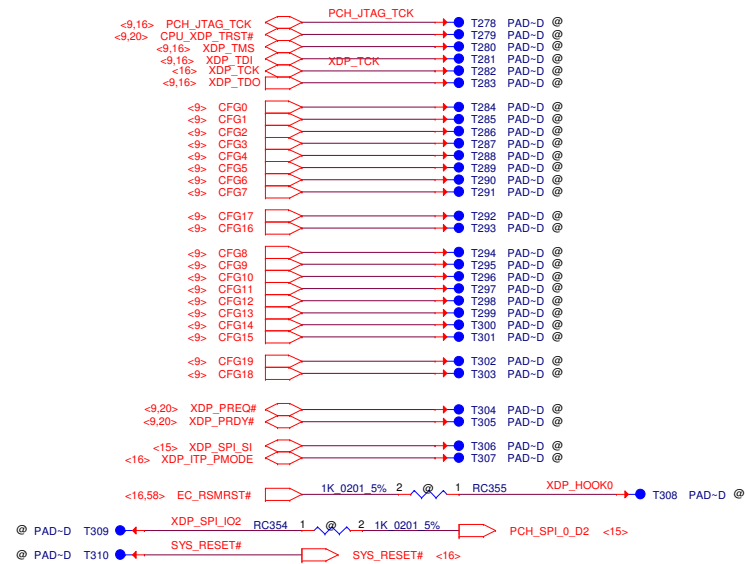
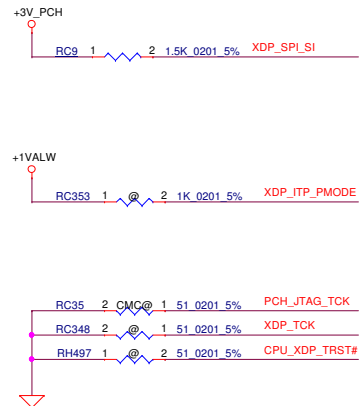
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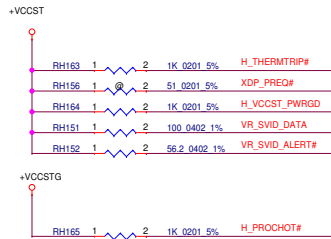


FOR TBT DD11

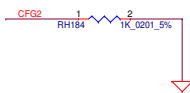


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				Date	Rev
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				Sheet	6 of 115

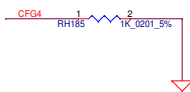




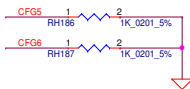
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



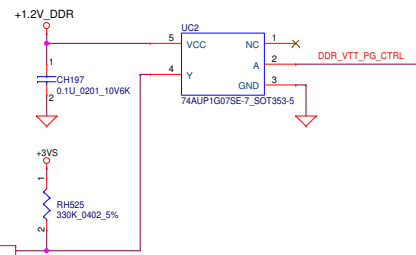
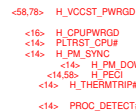
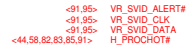
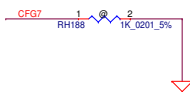
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port ★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



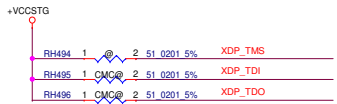
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) ★ 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



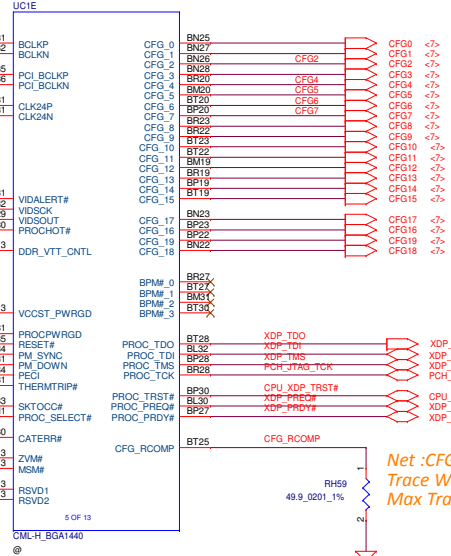
PEG DEFER TRAINING	
CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



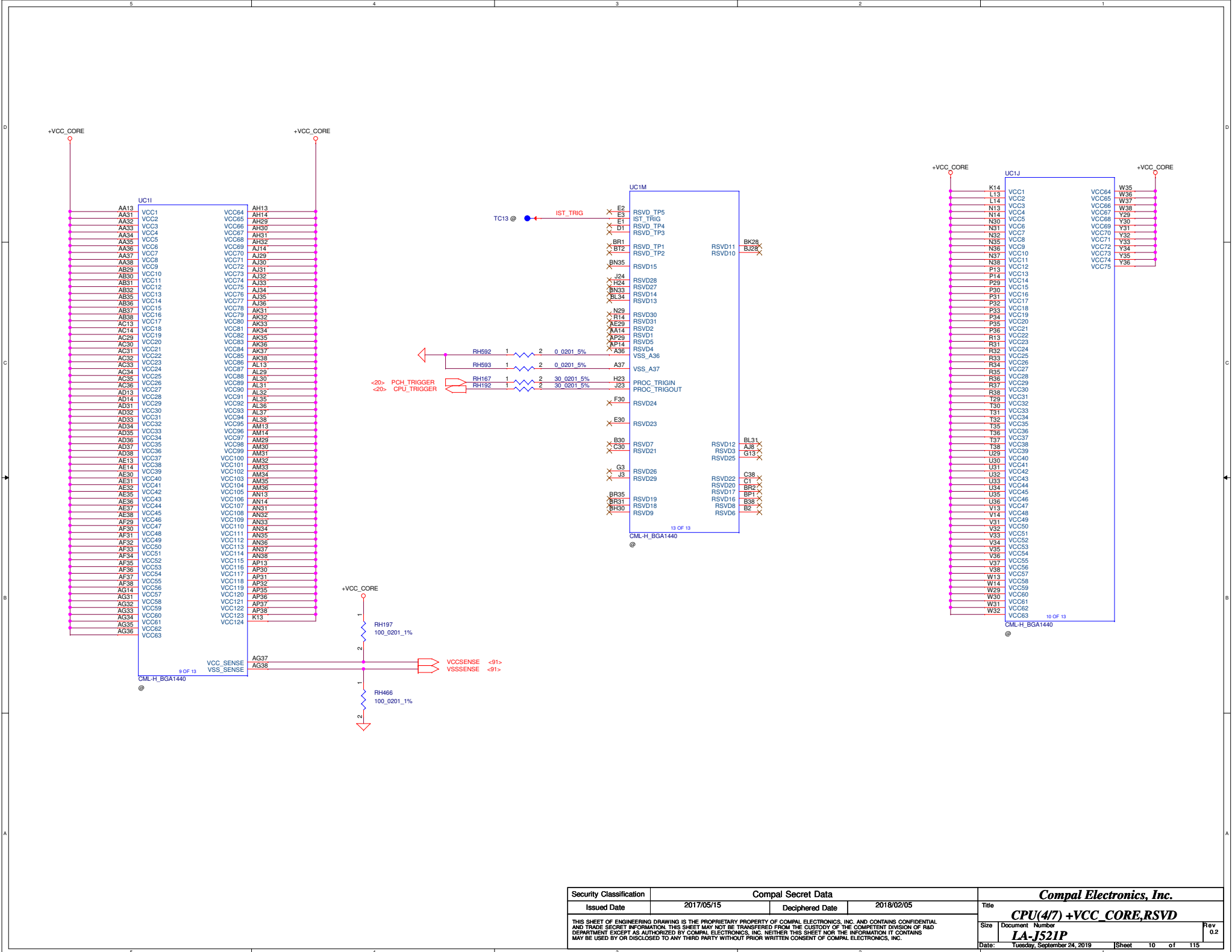
<87> SM_PG_CTRL



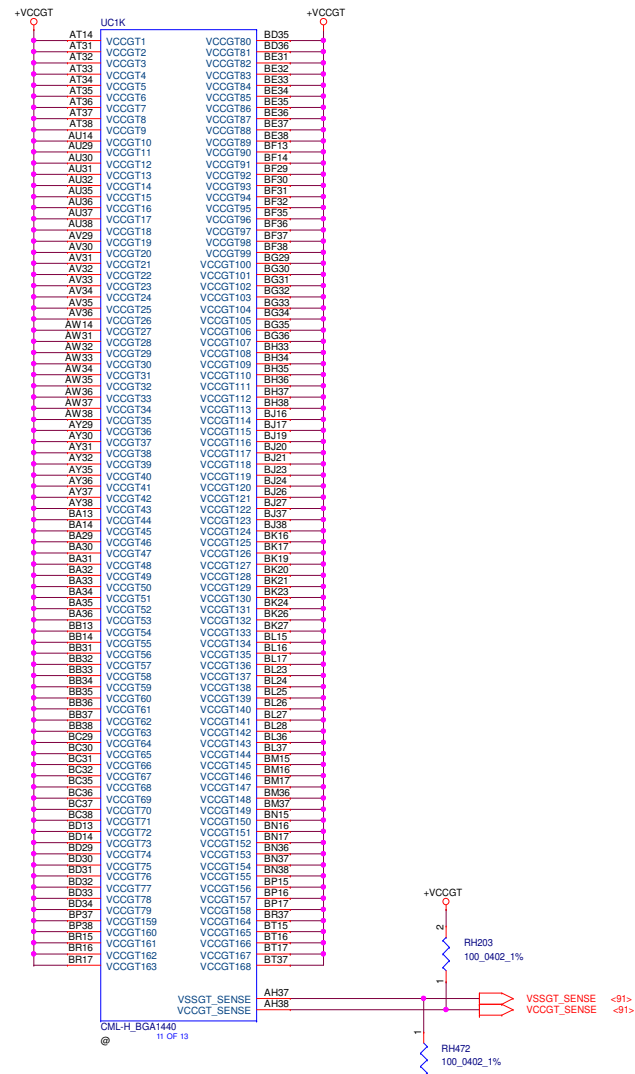
RH489,RH493 close to UH4



Net :CFG_RCOMP
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil



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Date:		Tuesday, September 24, 2018		Sheet 10 of 115	



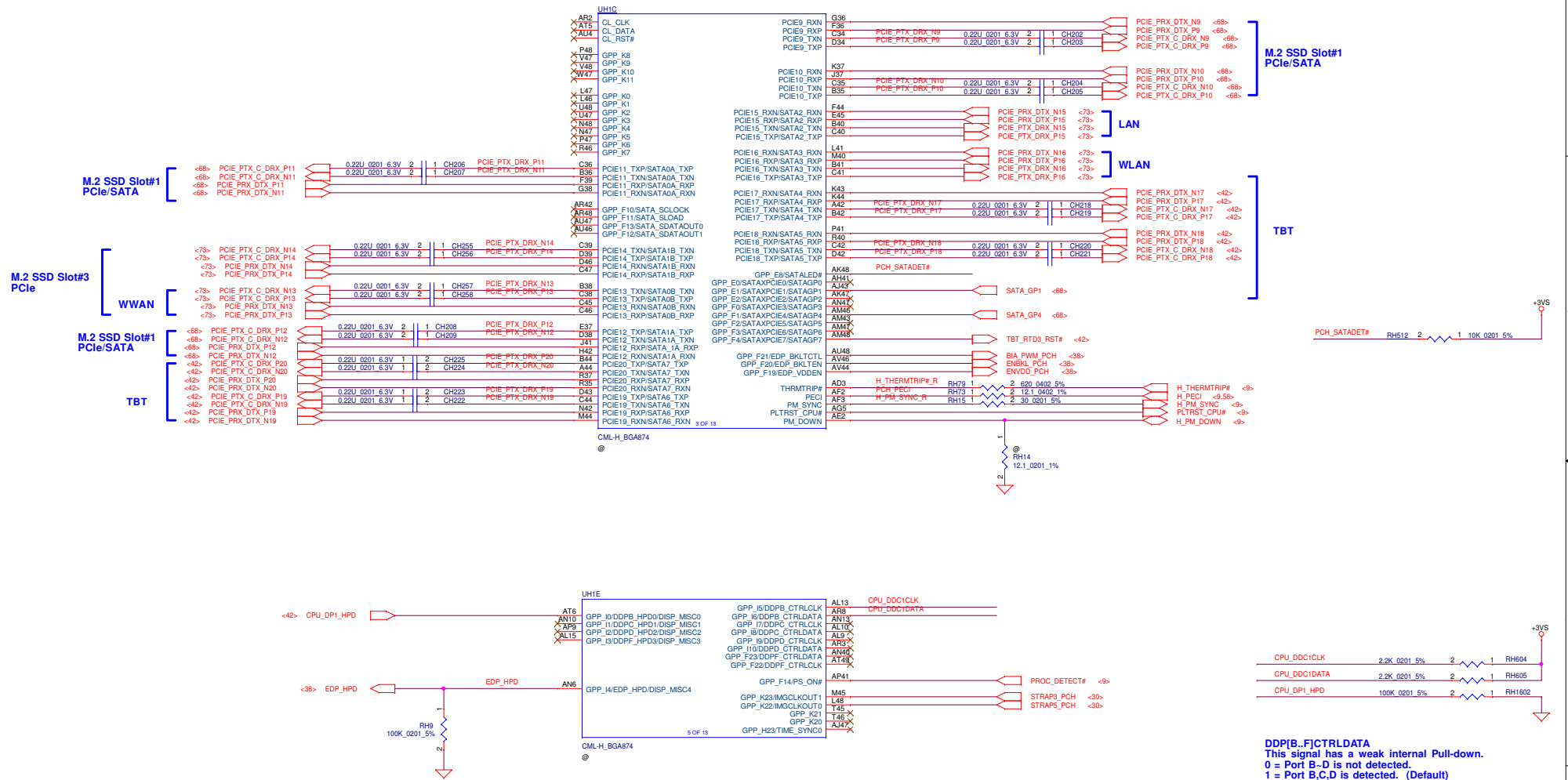
1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

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				Size	Document	Number			Rev	
				LA-J521P			0.2			
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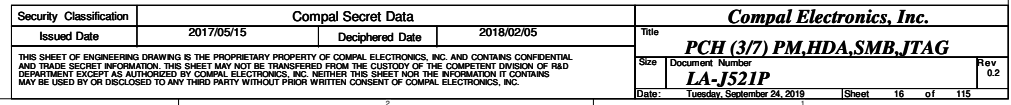
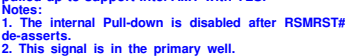


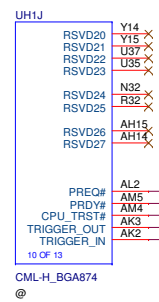
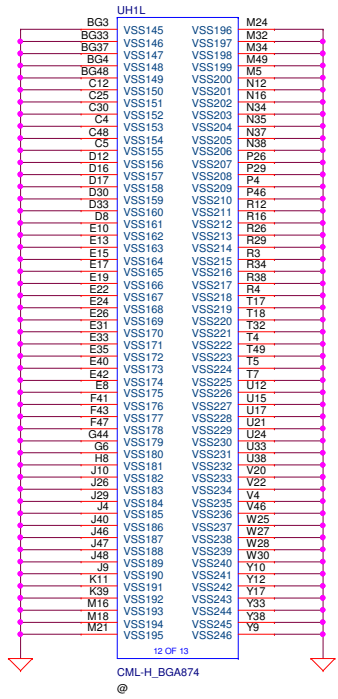
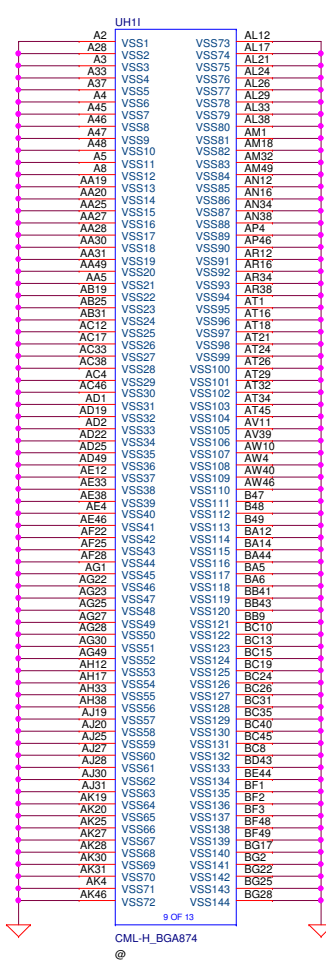
FHSSKU MBL QS64 A0 FCBGA 874P S
SA000003FOL
PCH@



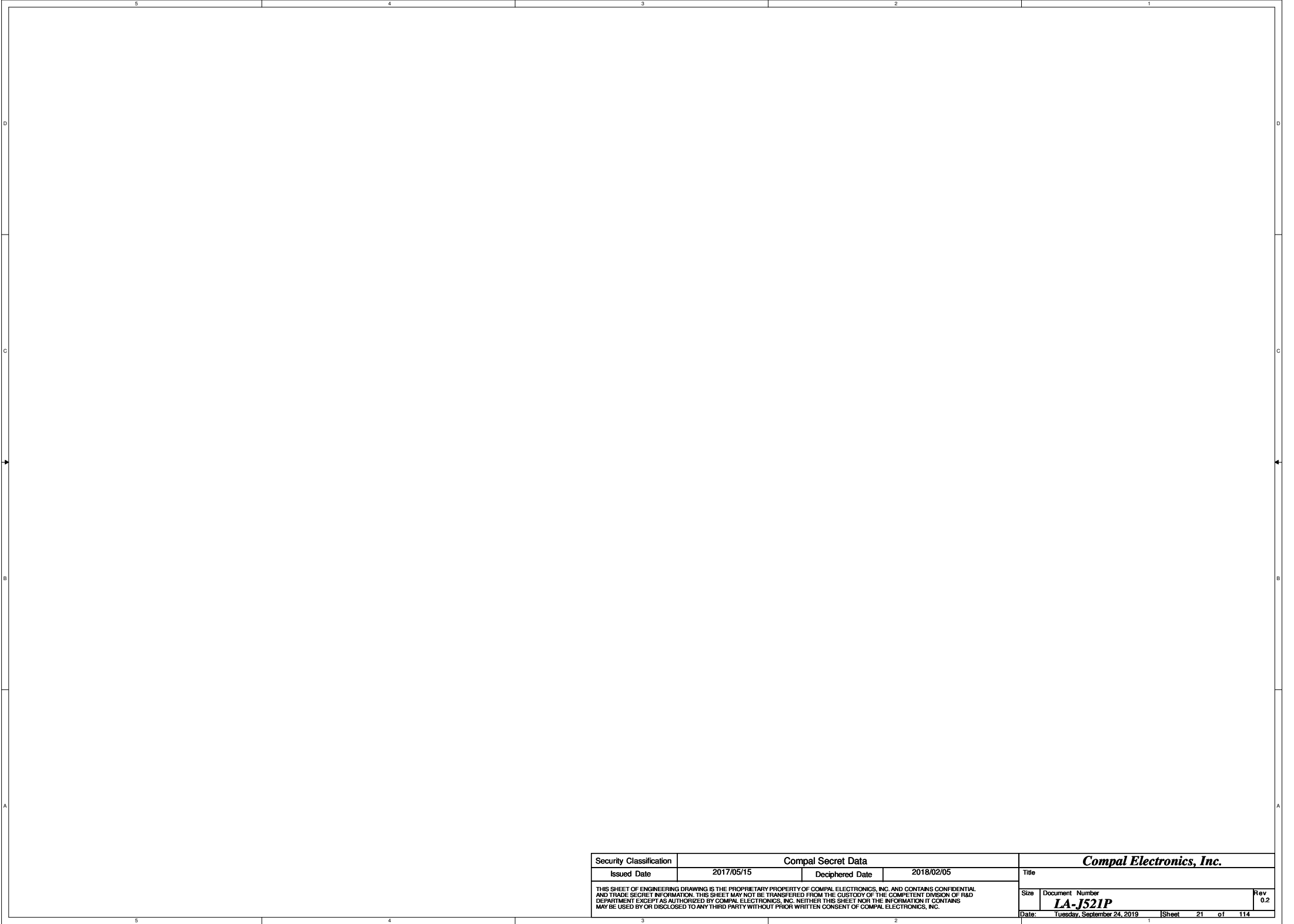
DDP[B.F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B-D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after PCH PWROK de-asserts.
2. This signal is in the primary well.

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Size	Document Number	Rev		0.2	
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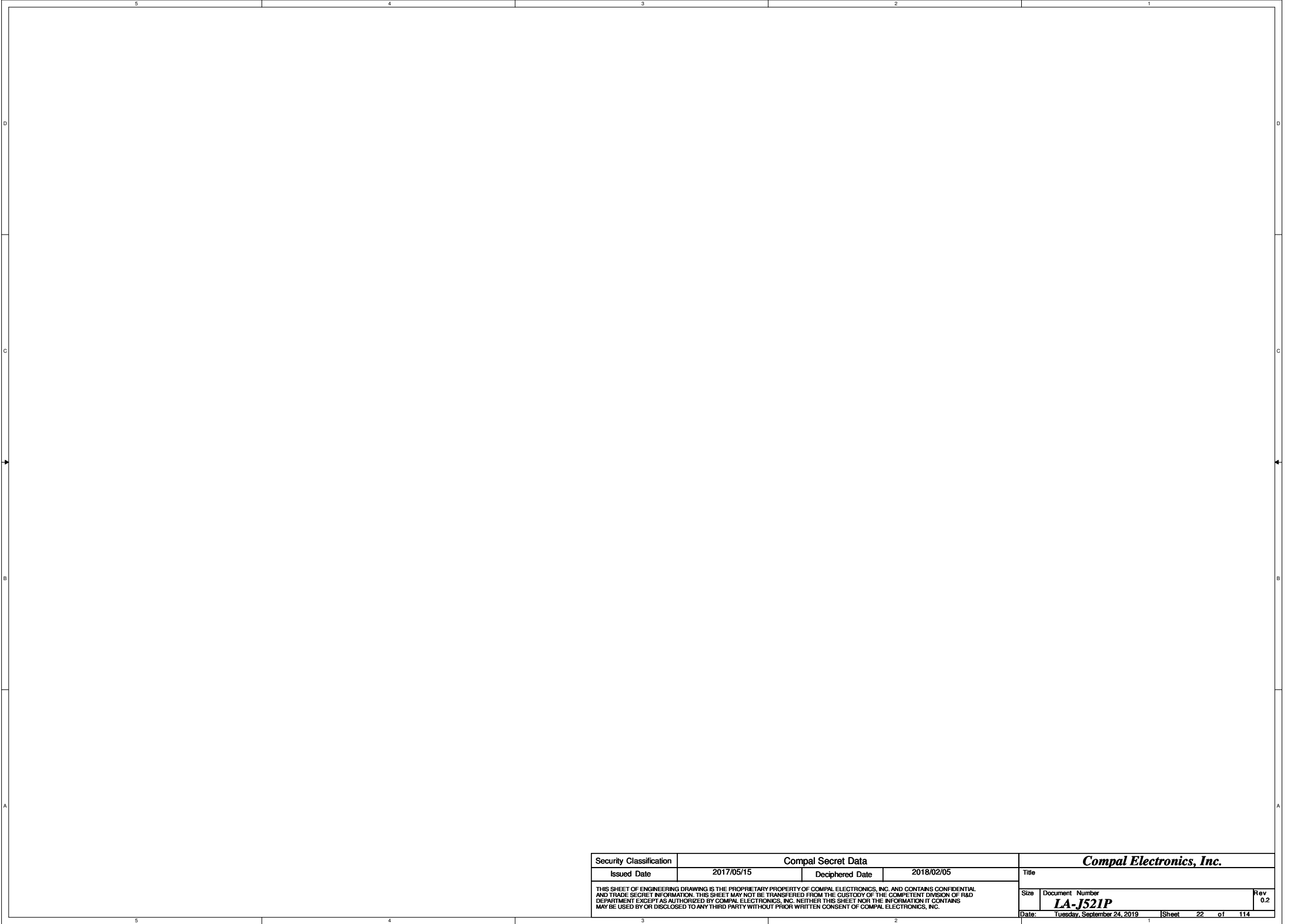




XDP_PREQ# <7,9>
XDP_PRODY# <7,9>
CPU_XDP_TRST# <7,9>
PCH_TRIGGER <10>
CPU_TRIGGER <10>

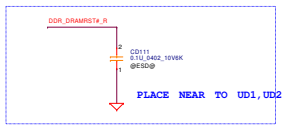
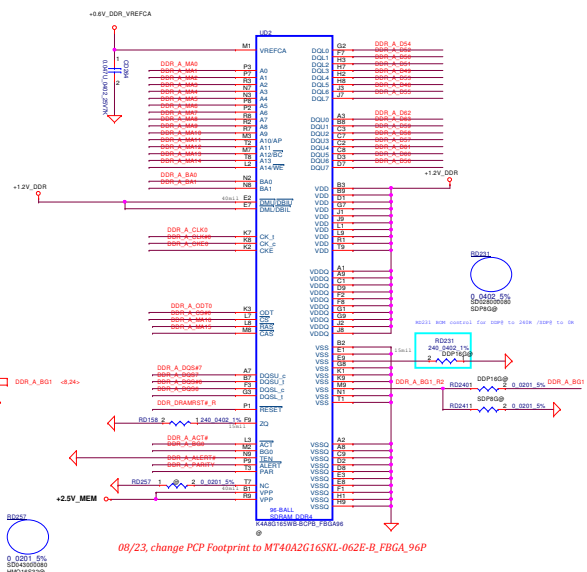
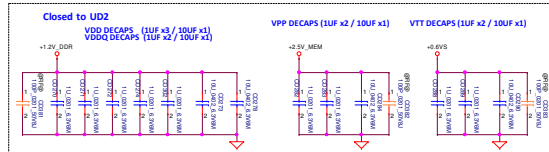


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Non-Interleave Memory



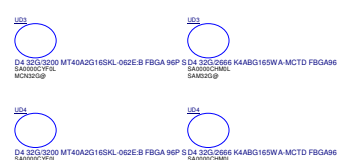
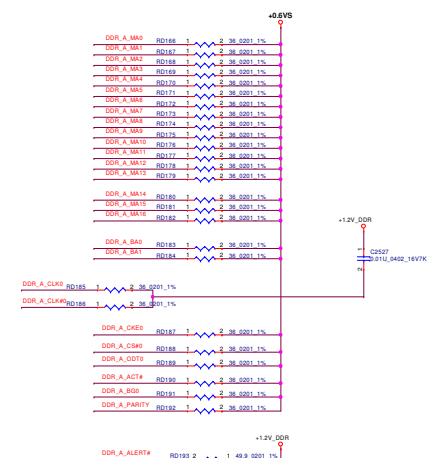
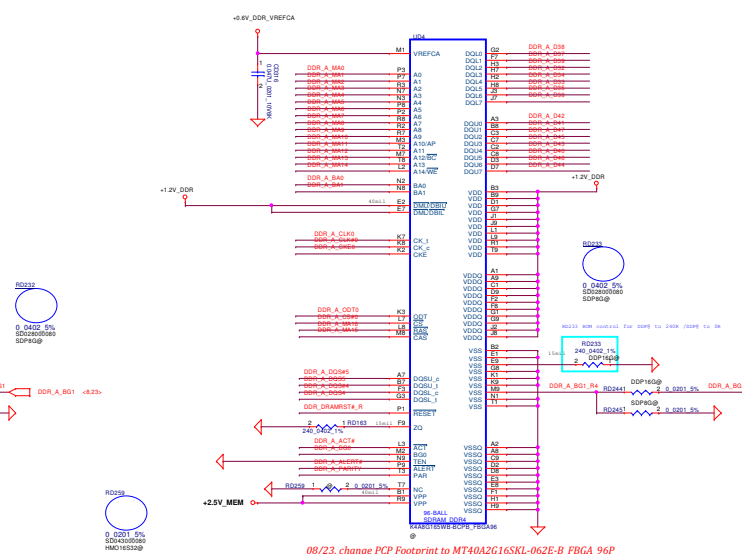
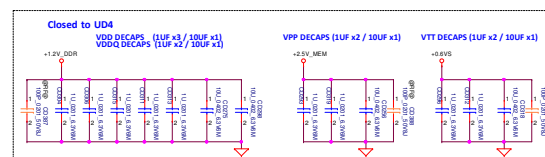
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			DDRA Memory Down CHA	
			LA-521P	
			Created	Issued
			2017/04/07	2018/12/01
			Page	23 of 115

<S.23> DDR_A_MA[0..16]

<S.23> DDR_A_DQS[0..7]

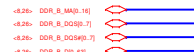
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<S.23> DDR_A_DQS[63]

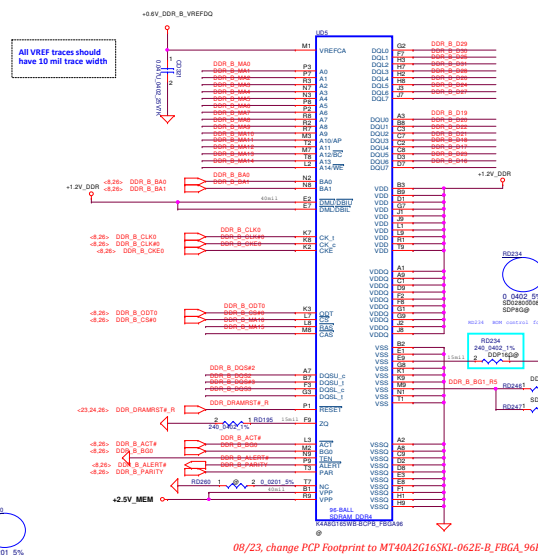
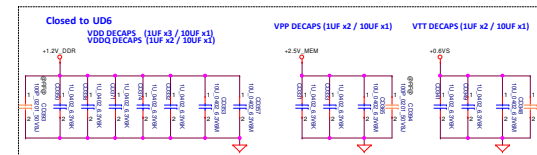
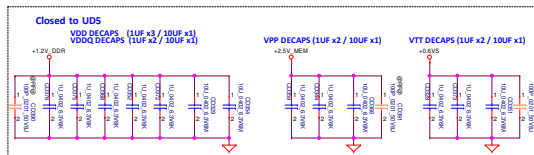
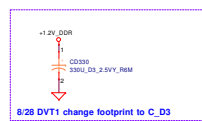
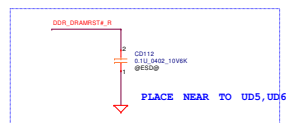
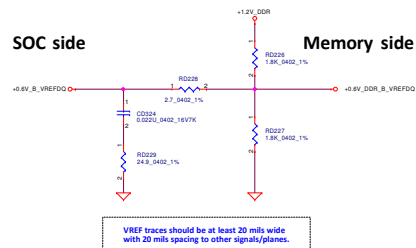


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Issued Date	2017/04/07	Declassified Date	2018/12/31	
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Date			2017/04/24	2018/02/24
Page			24	113

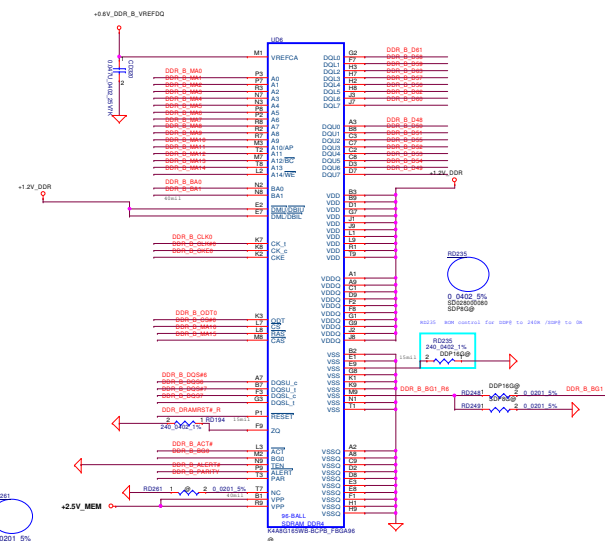
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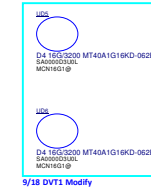
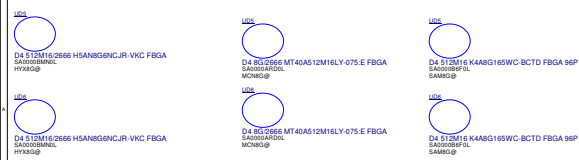
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08/23, change PCP Footprint to MT40A2G16SKL-062E-B_FBGA_96F

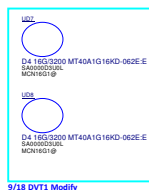
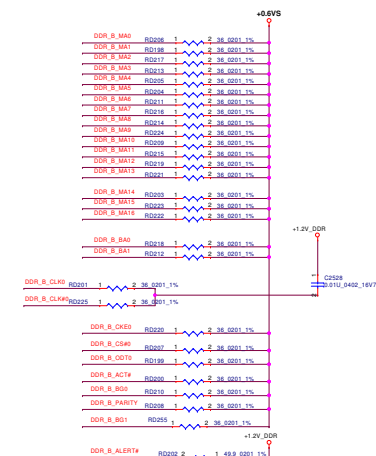
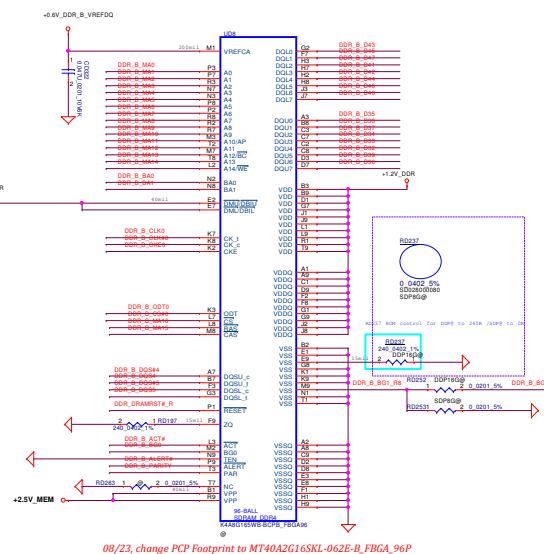
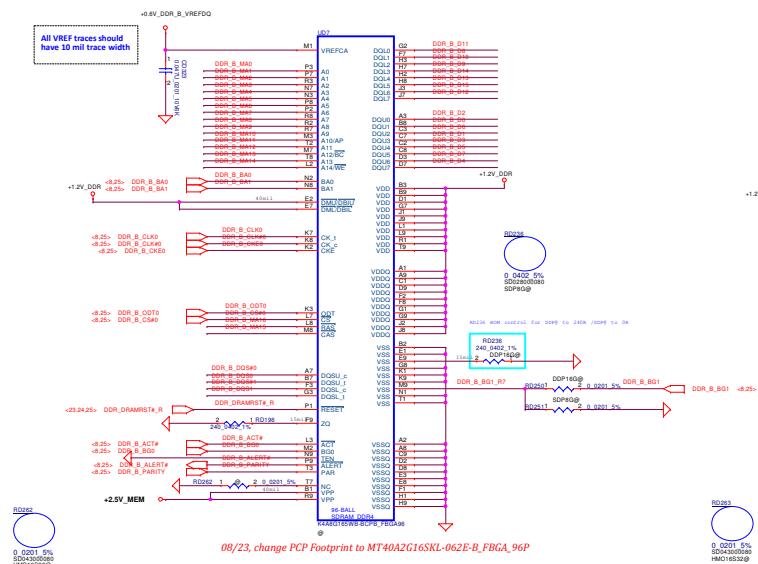
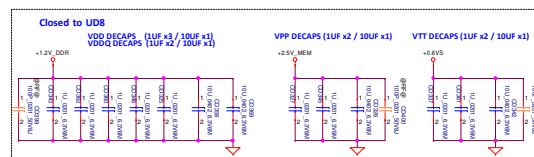
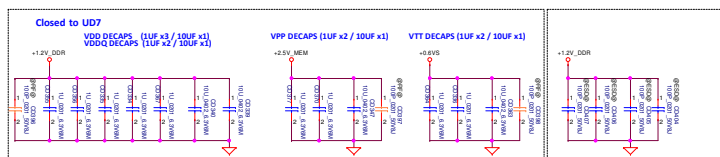


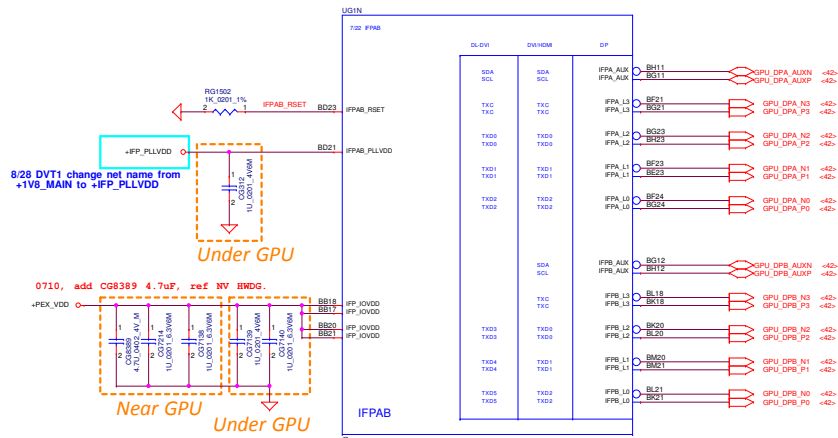
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Date 2017/04/07		Issued Rev. 01 of 01	Rev

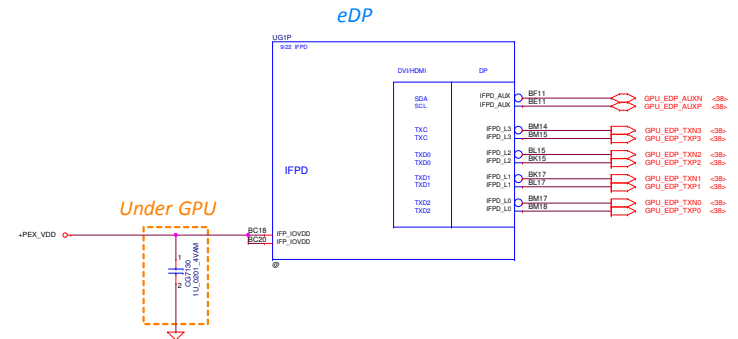
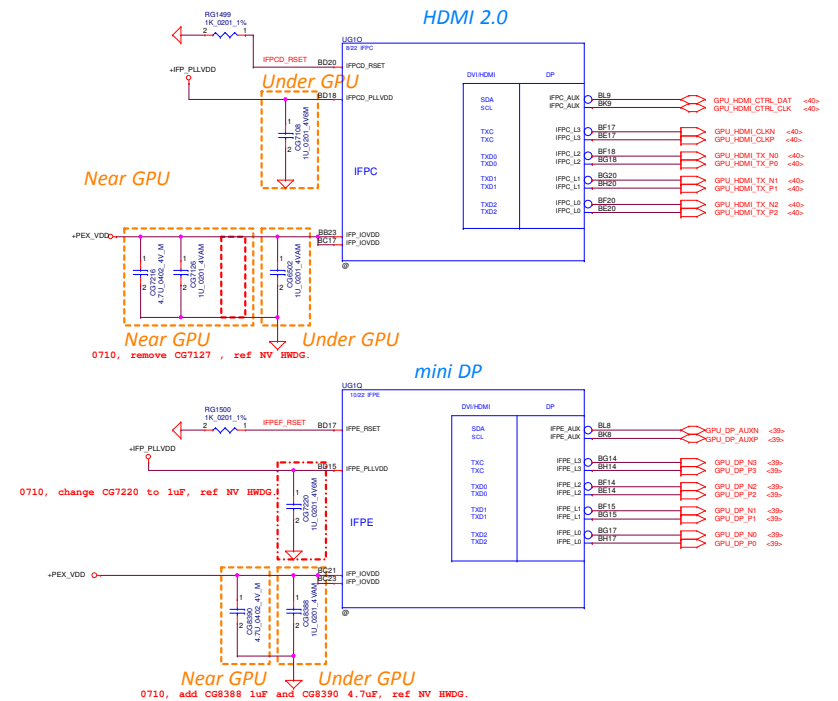
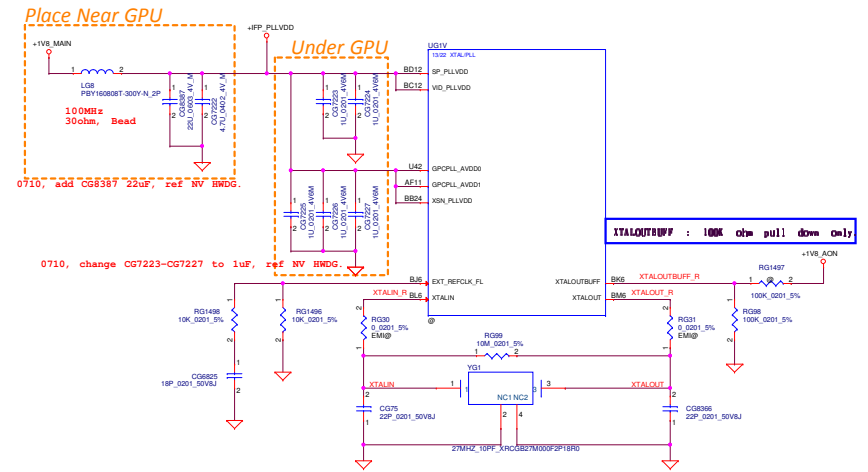
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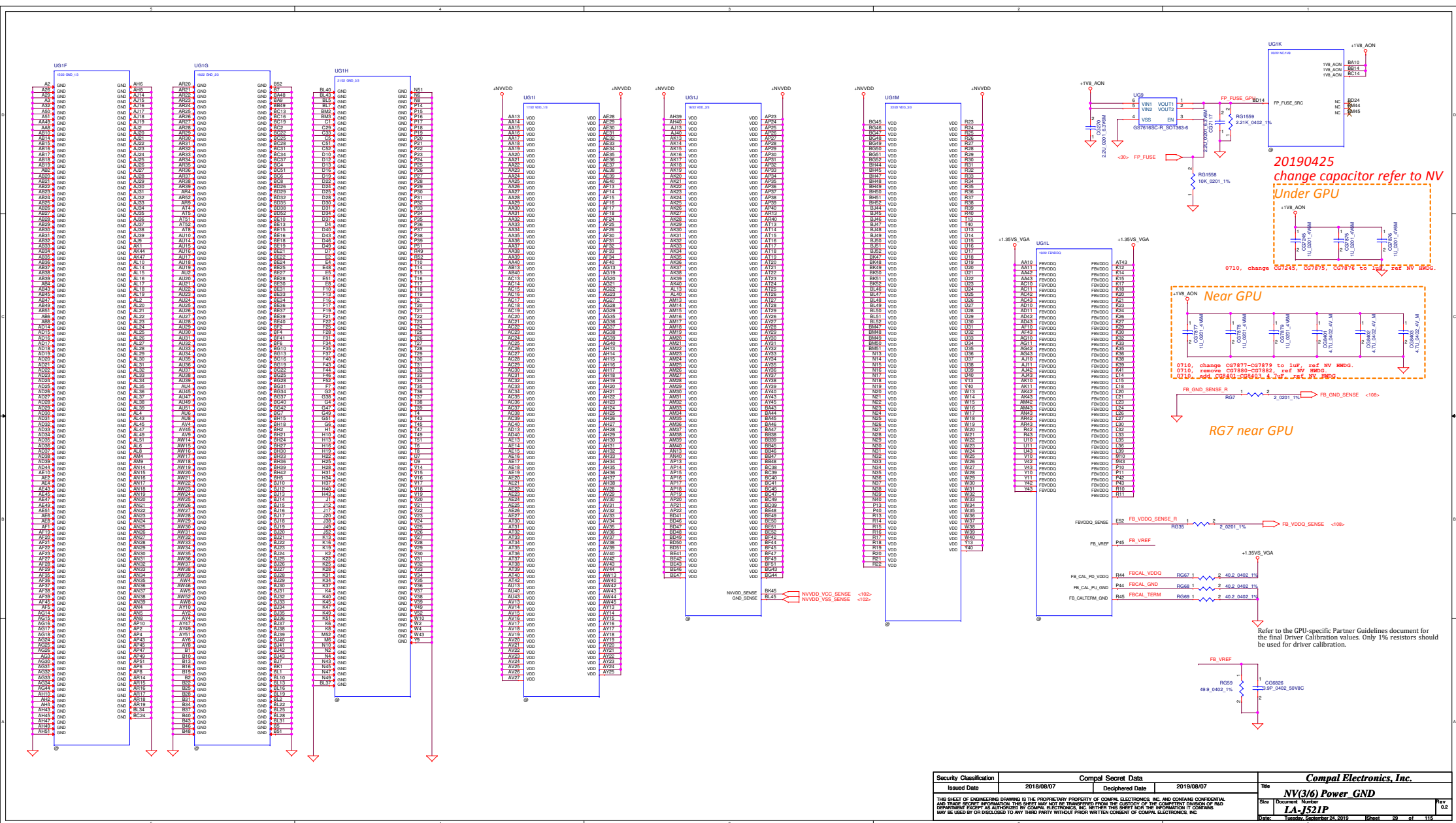


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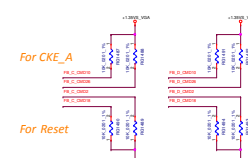
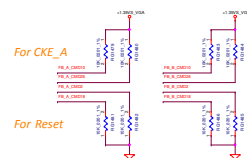
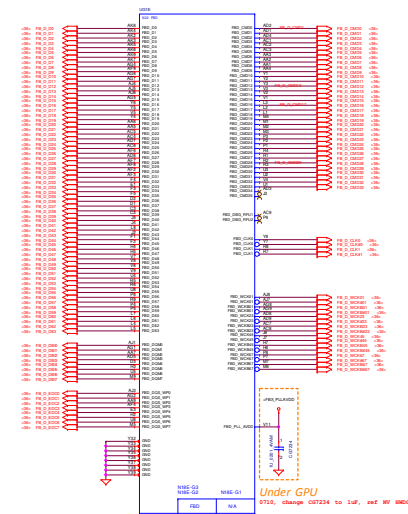
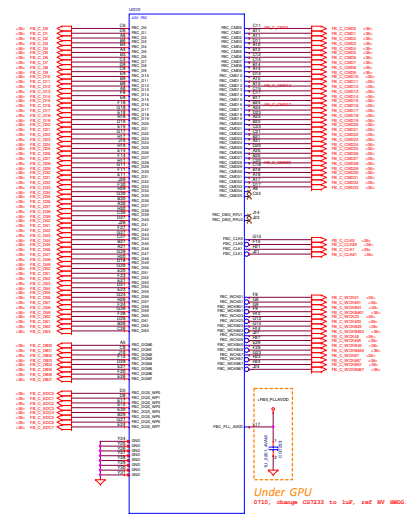
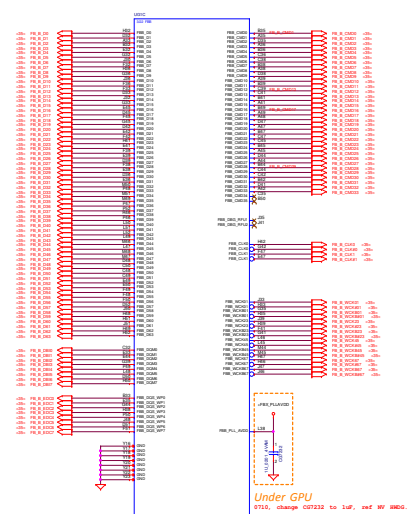
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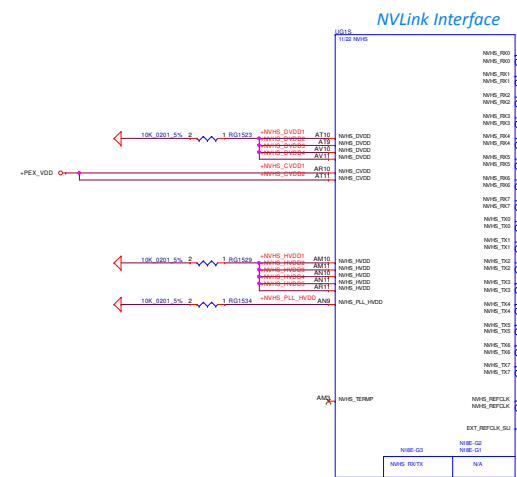
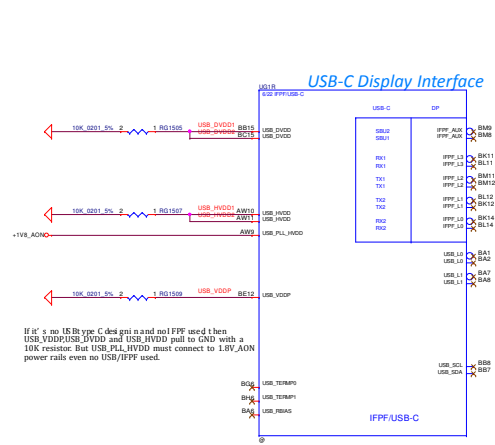


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NV(2/6) IFP ABCDEF DAC XTAL				0.2
LA-J521P				Rev
Date: Tuesday, September 25, 2019				Sheet 28 of 115



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/08/07	Deciphered Date	2019/08/07	Title	NV3(6) Power GND
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				Date	LA-5212P
				Date	Jan 29, 2019
				Sheet	29 of 115
				Rev	0.2



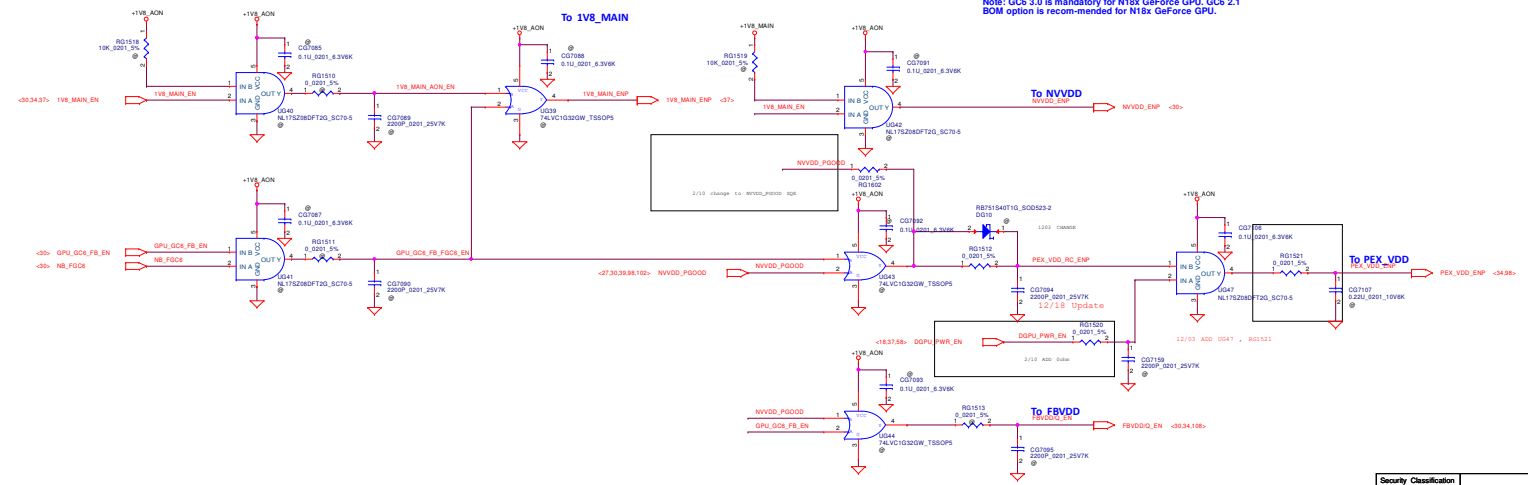


N18E GPU does not support NVLink. Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, NVHS_PLL_HVDD rails to GND with 10K Resistor. Do not use any decoupling or filtering capacitor for NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, NVHS_PLL_HVDD rails. Leave NVHS_TERM, EXT_REFCLK_SUI, NVHS_REFCLK, NVHS_TX and NVHS_RX signals floating (NC)."

FGC6 Reserved

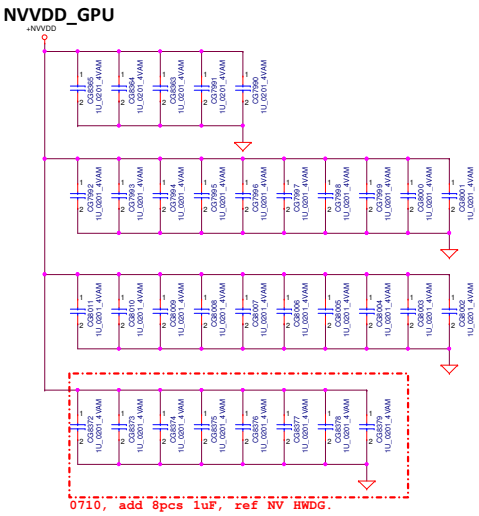
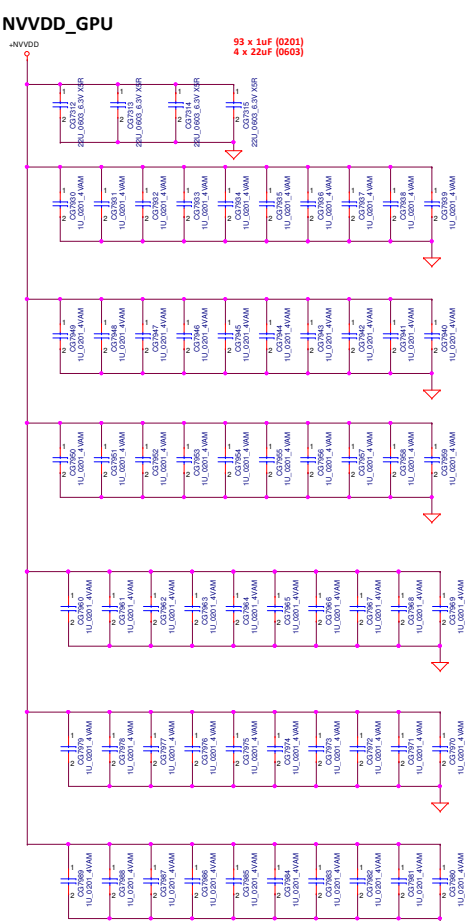
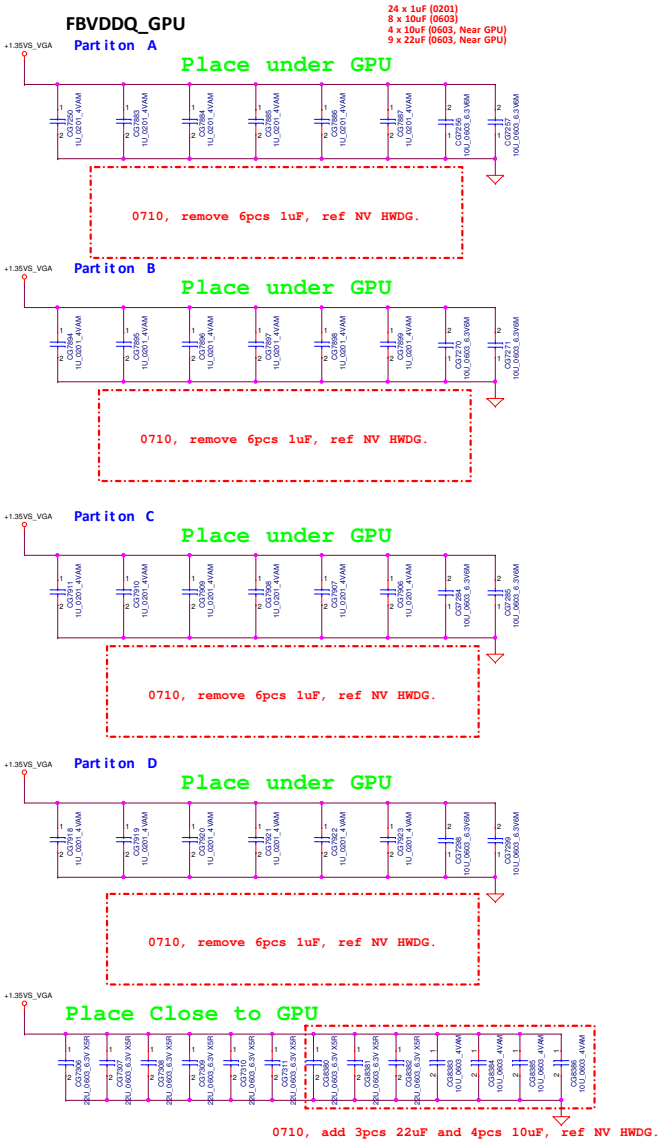
Reference board power seq. will handle by PMU. Therefore demo circuit will have other power path to control the FGC6 or other GPU power seq. QDM must associate FGC6 power circuit includes power on/off into its owned circuit.

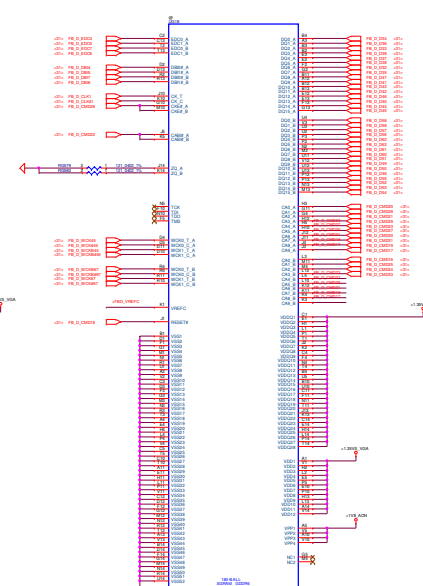
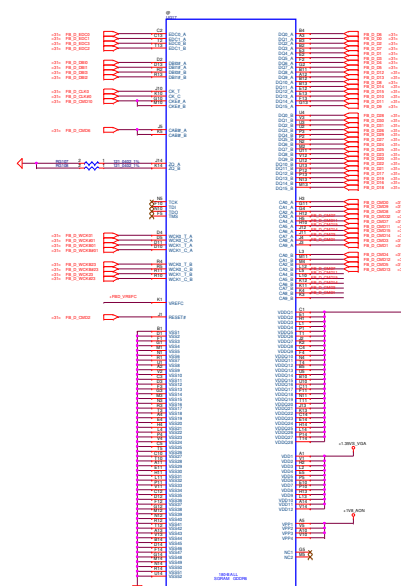
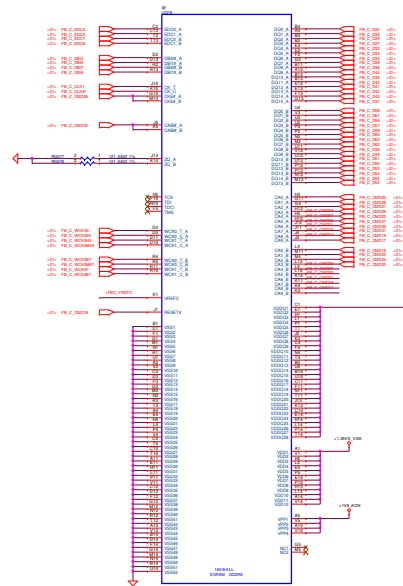
Note: GC6 3.0 is mandatory for N18x GeForce GPU. GC6 2.1 BOM option is recom-mended for N18x GeForce GPU.



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				Rev	0.2
				Drawn	1/2/2018
				Checked	1/2/2018
				Approved	1/2/2018
				Page	10 of 115

GPU Decoupling - NV Spec Recommendation

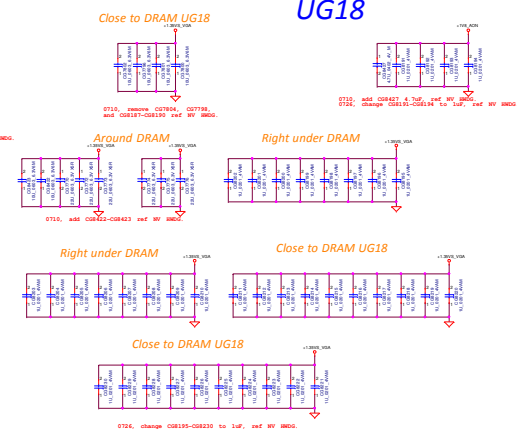
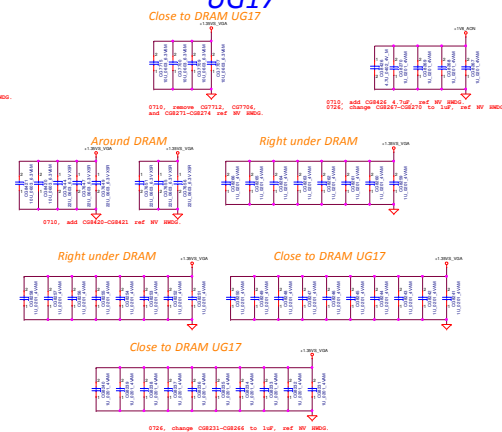
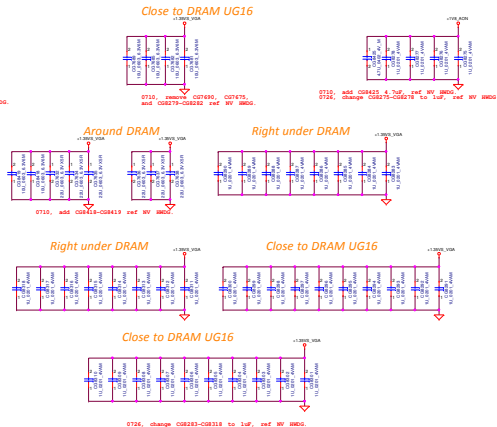
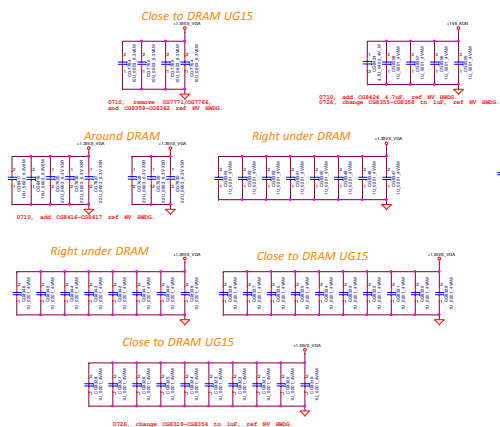


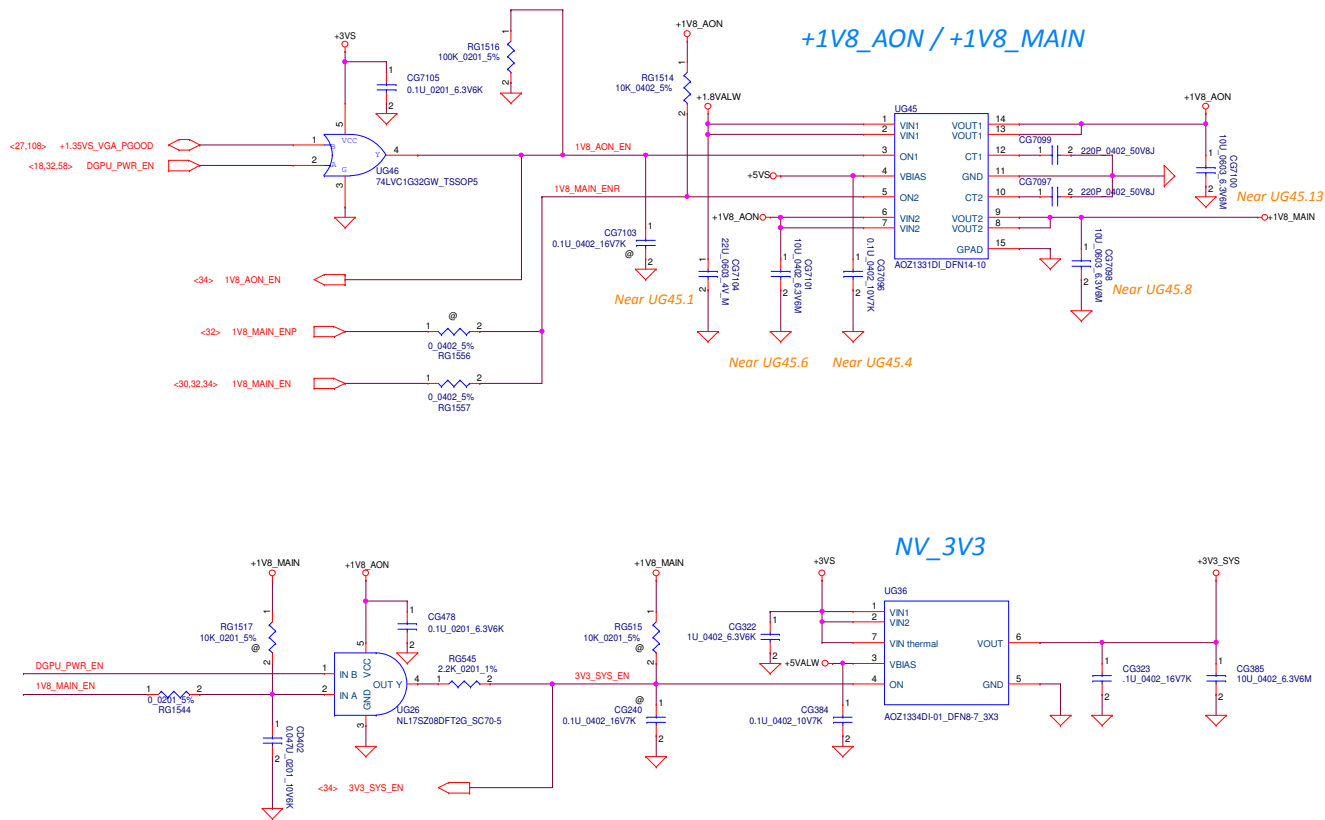


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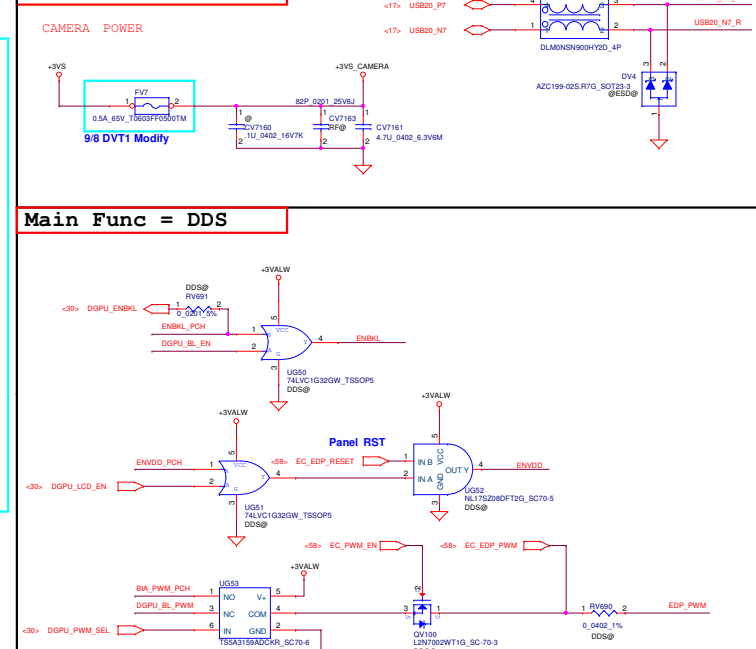
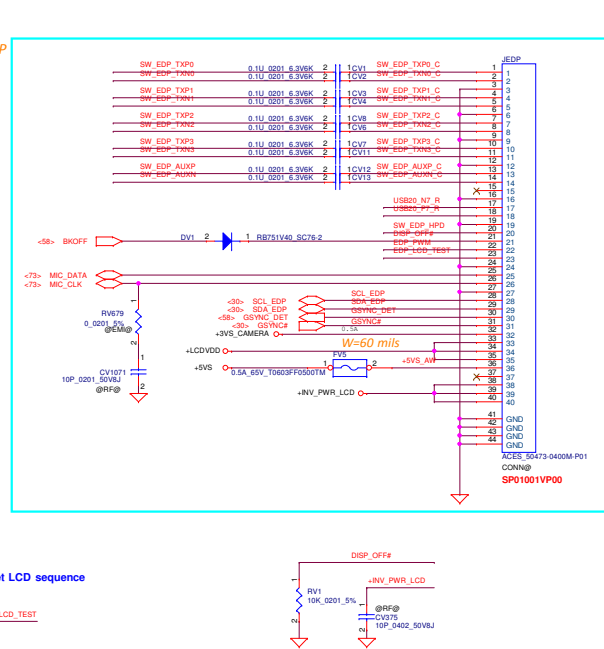
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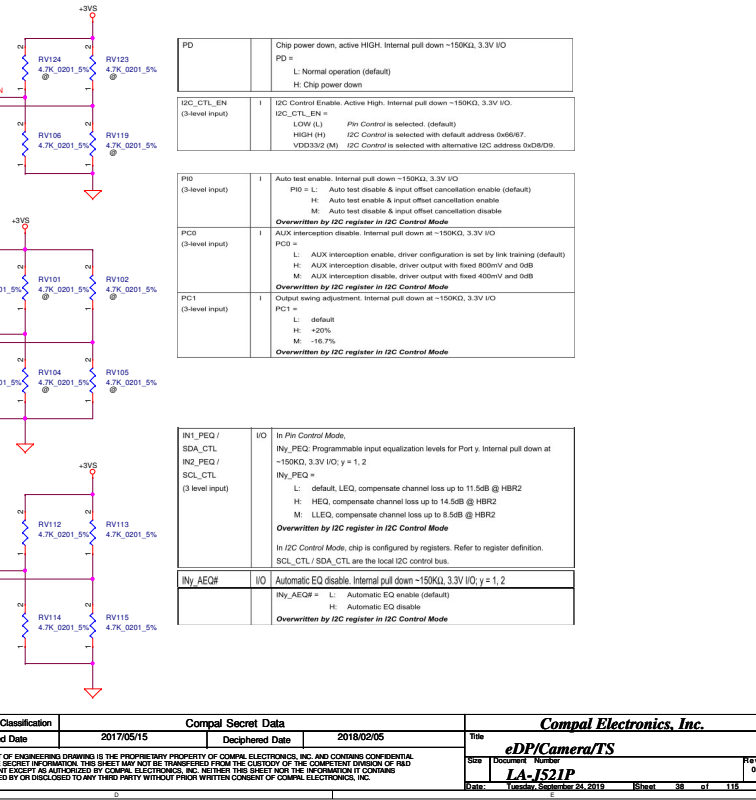
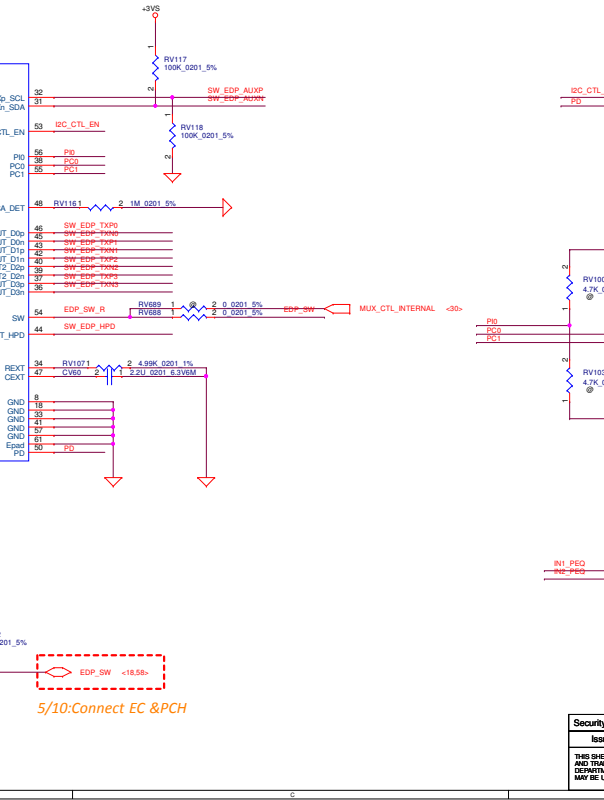




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					LA-J521P
				Date:	Tuesday, September 24, 2019
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				Rev	0.2

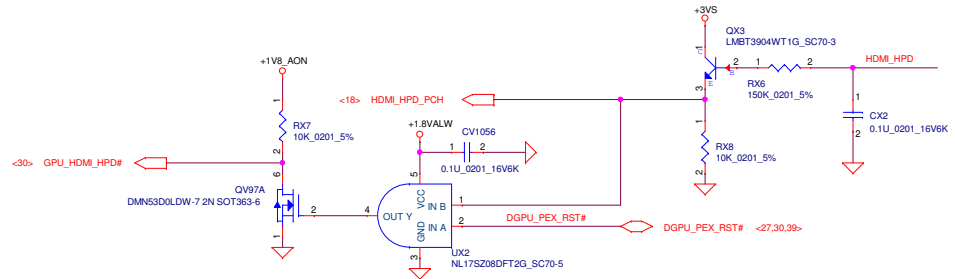
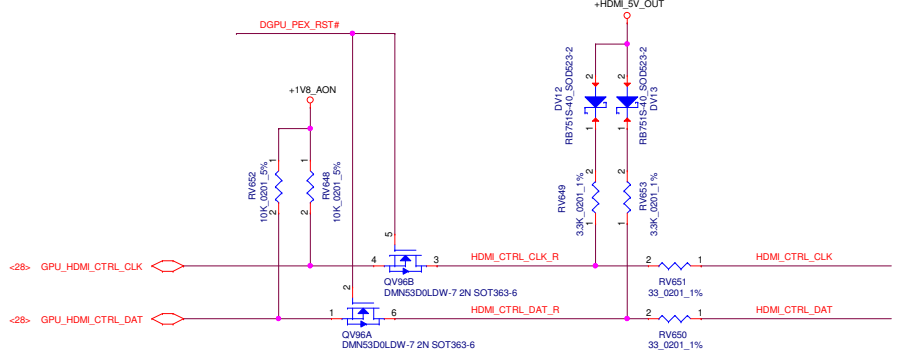
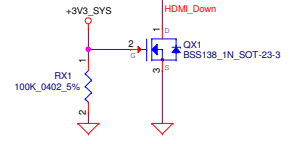
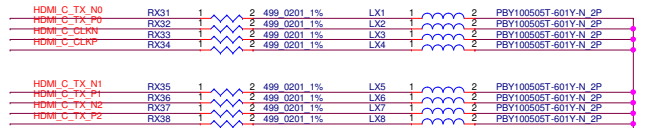
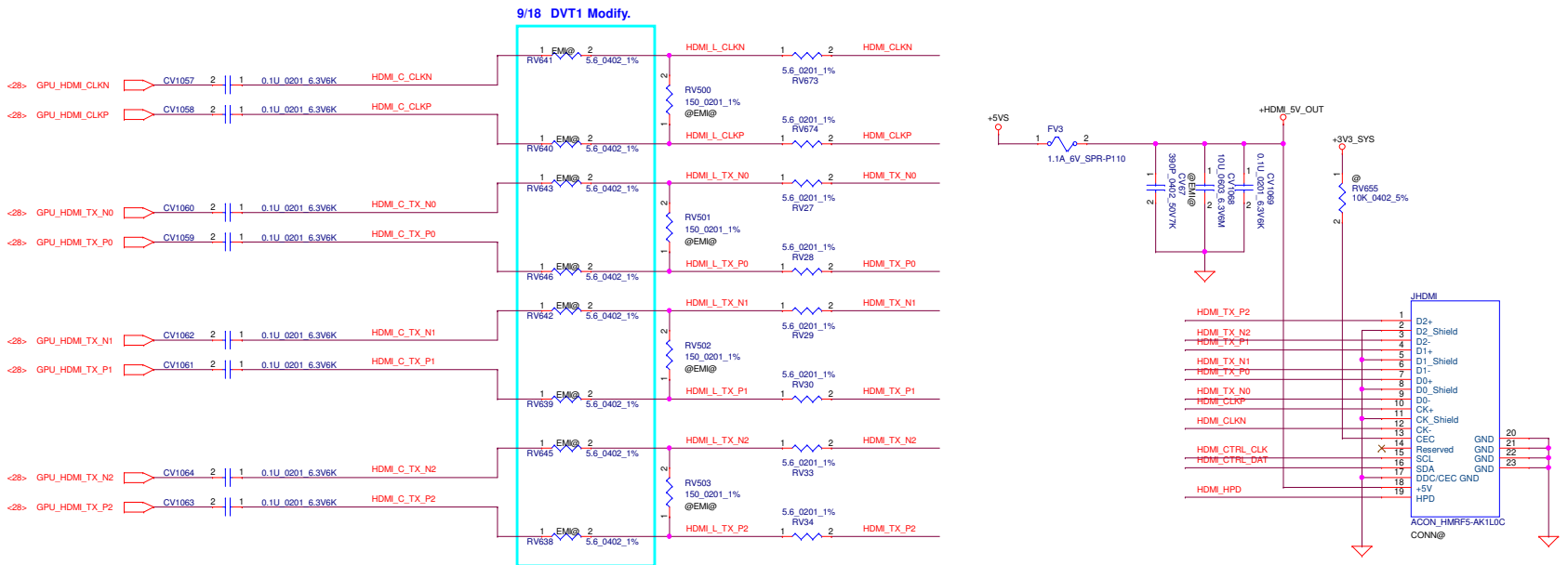
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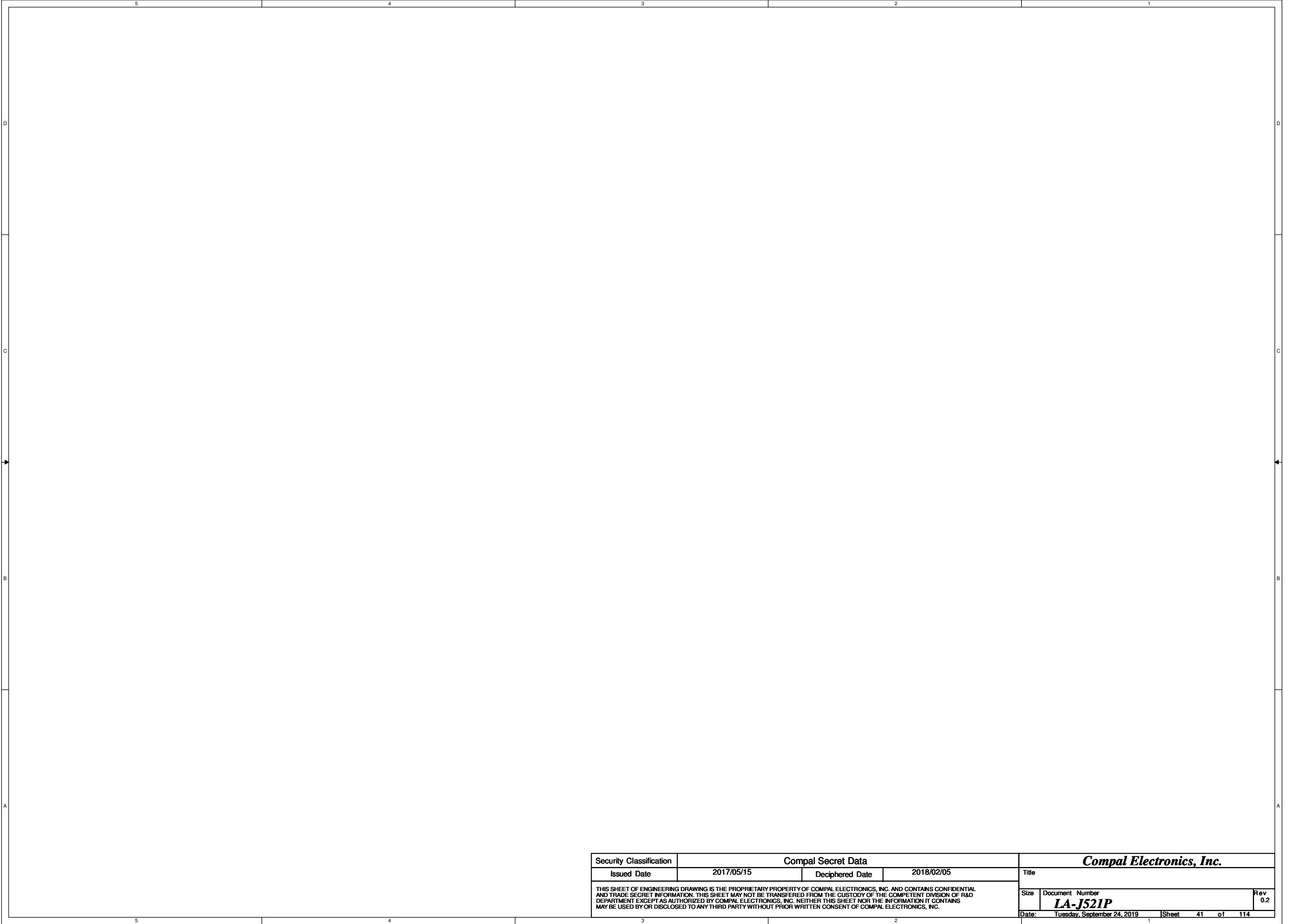




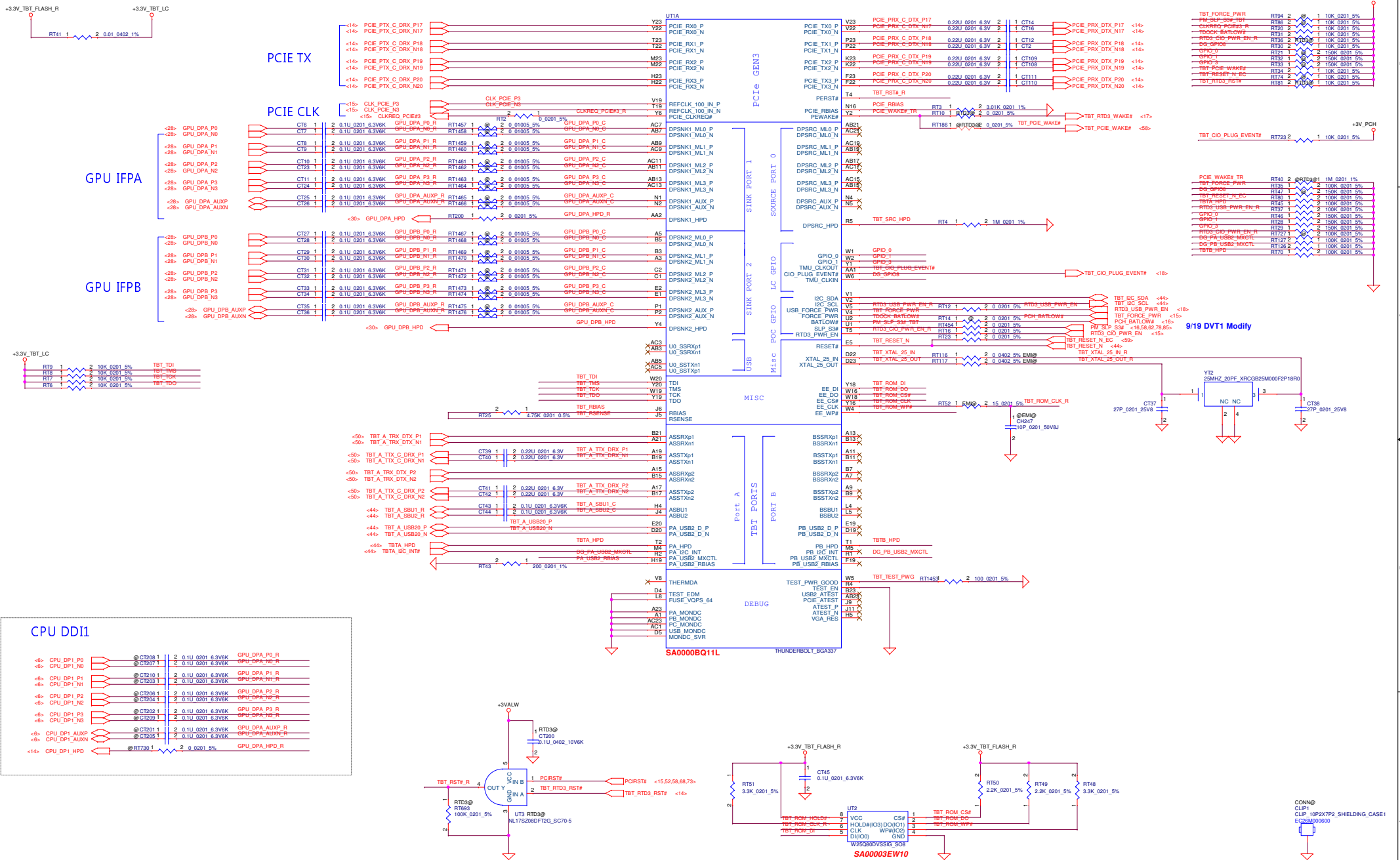
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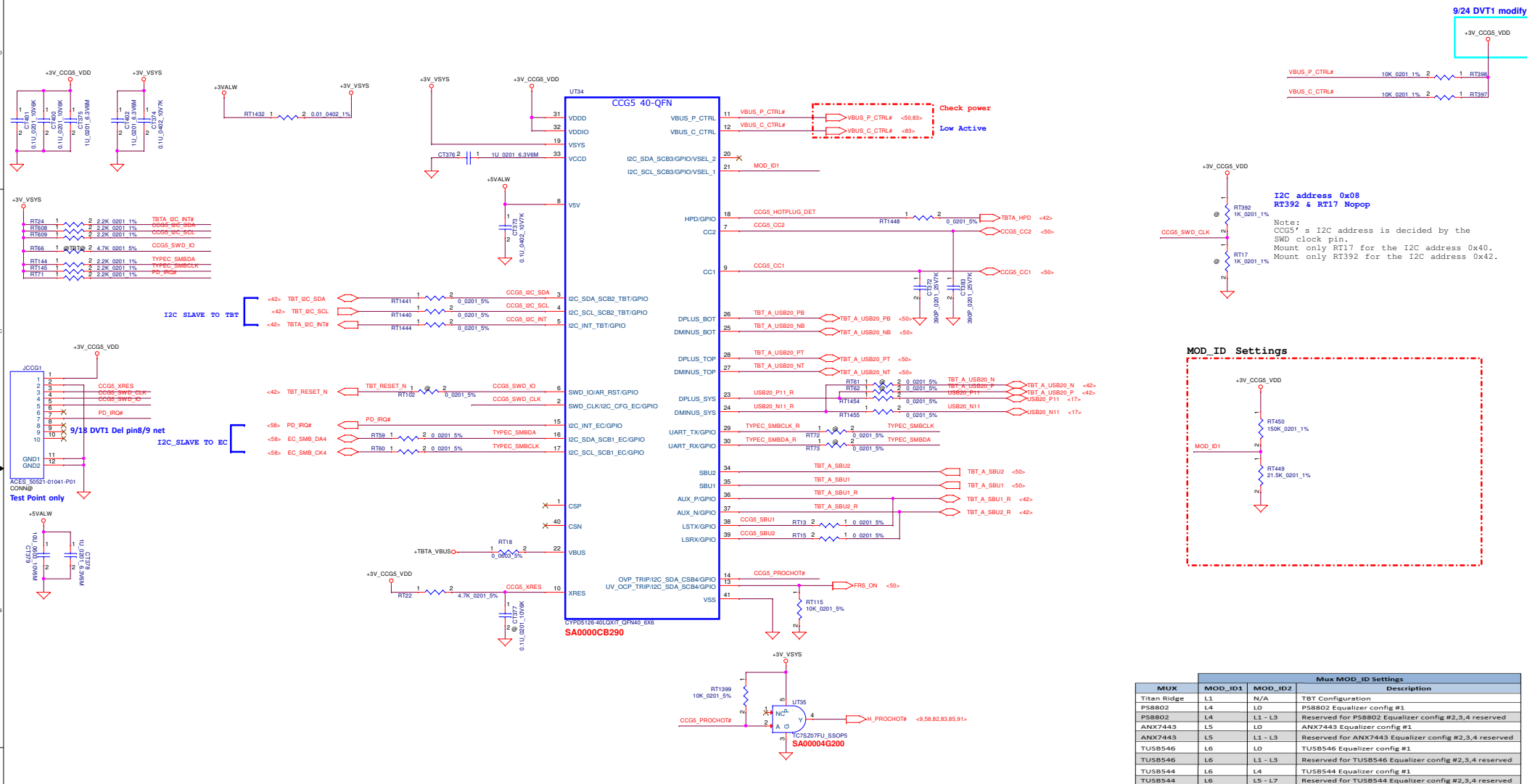
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Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title	eDP/Compal/TS
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Date	1/24/2019			Sheet	08 of 115



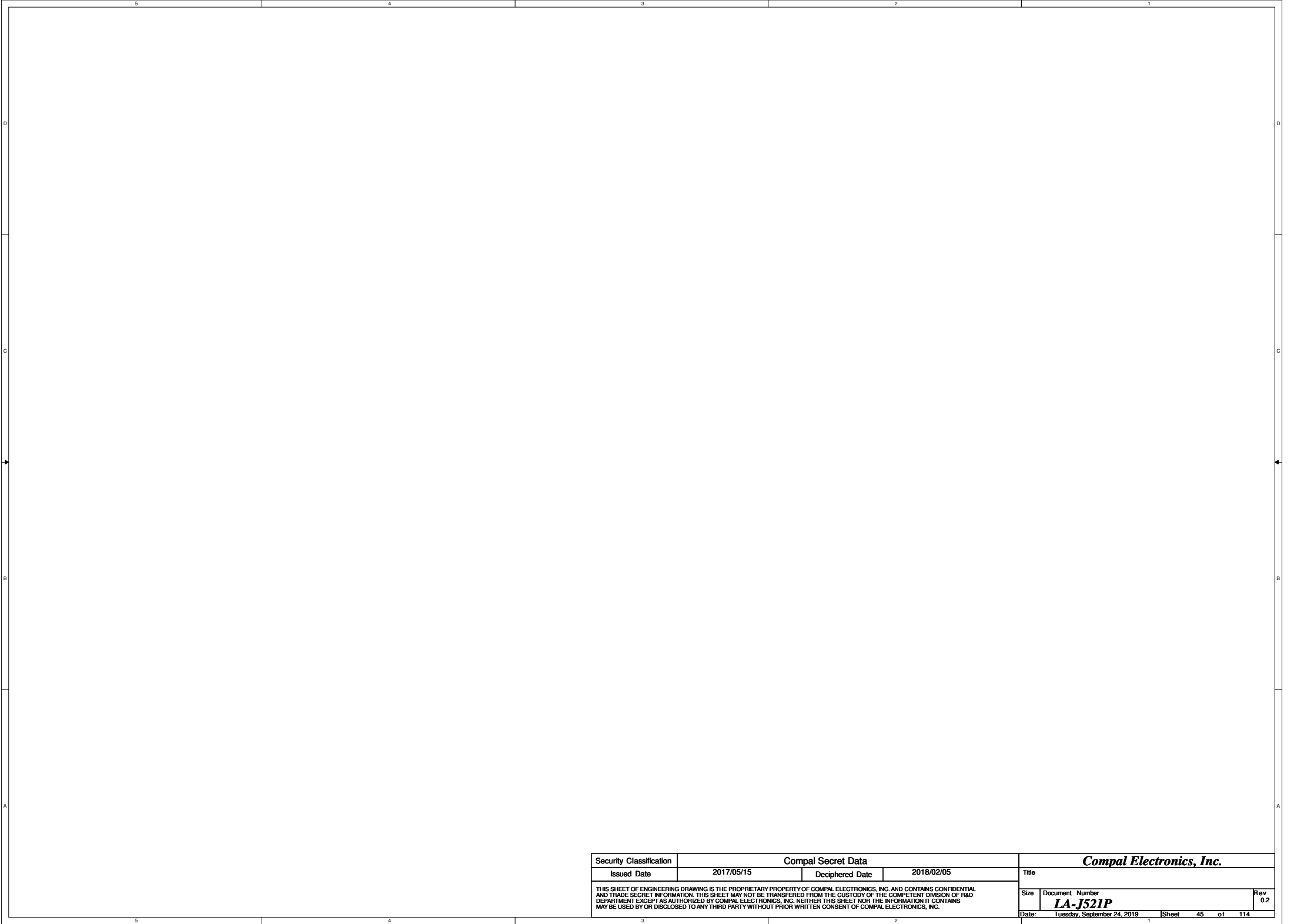


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Date: Tuesday, September 24, 2019		Sheet		41	of 114

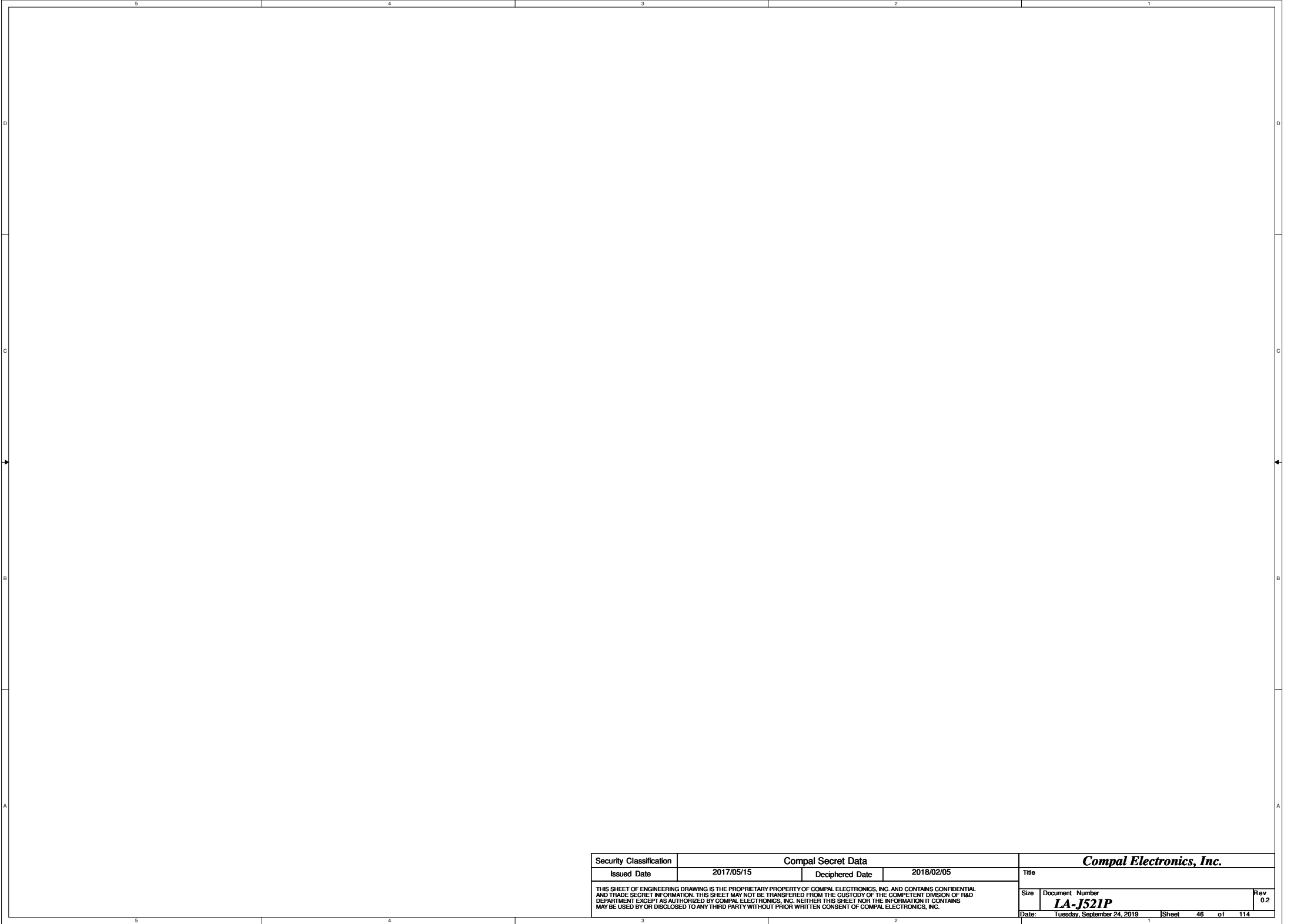




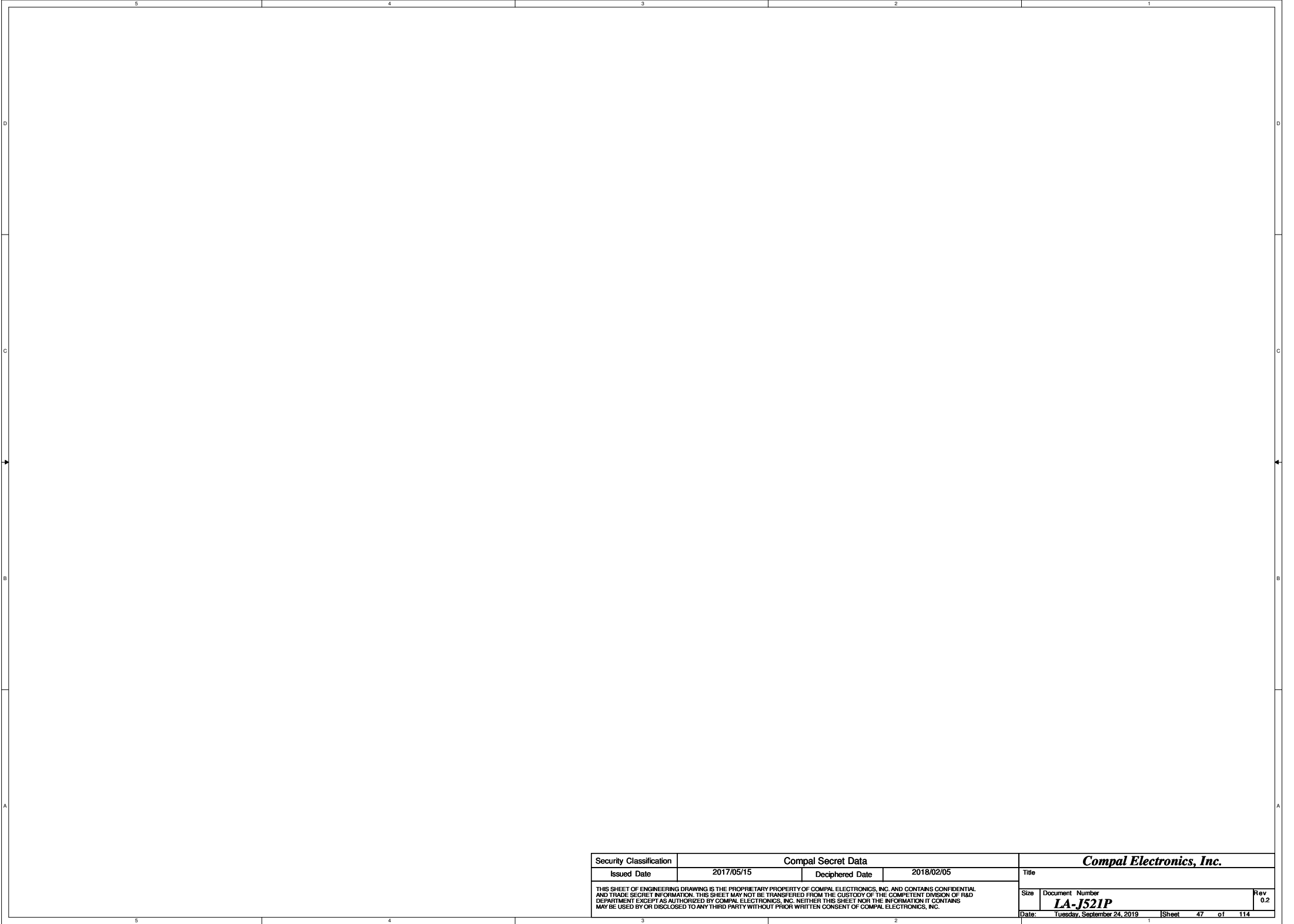
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Titan Ridge	L1	N/A	TBT Configuration
PS8B02	L4	L0	PS8B02 Equalizer config #1
PS8B02	L4	L1 - L3	Reserved for PS8B02 Equalizer config #2,3,4 reserved
ANK7443	L5	L0	ANK7443 Equalizer config #1
ANK7443	L1 - L5	L1 - L3	Reserved for ANK7443 Equalizer config #2,3,4 reserved
TUS5B46	L6	L0	TUS5B46 Equalizer config #1
TUS5B46	L6	L1 - L3	Reserved for TUS5B46 Equalizer config #2,3,4 reserved
TUS5B44	L6	L4	TUS5B44 Equalizer config #1
TUS5B44	L6	L5 - L7	Reserved for TUS5B44 Equalizer config #2,3,4 reserved



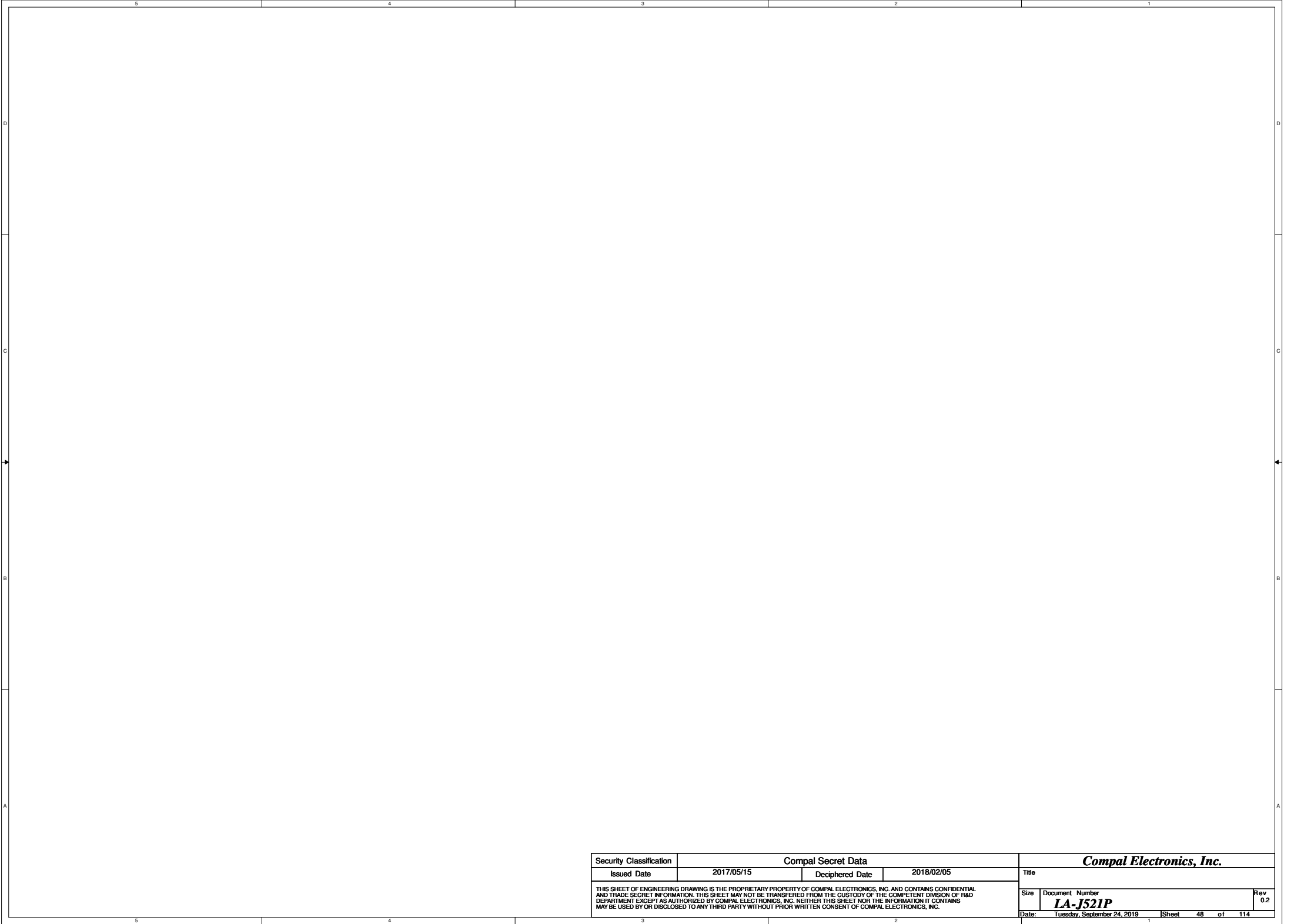
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											<i>LA-J521P</i>			0.2	
								Date: Tuesday, September 24, 2019							
						Sheet 45		of 114							



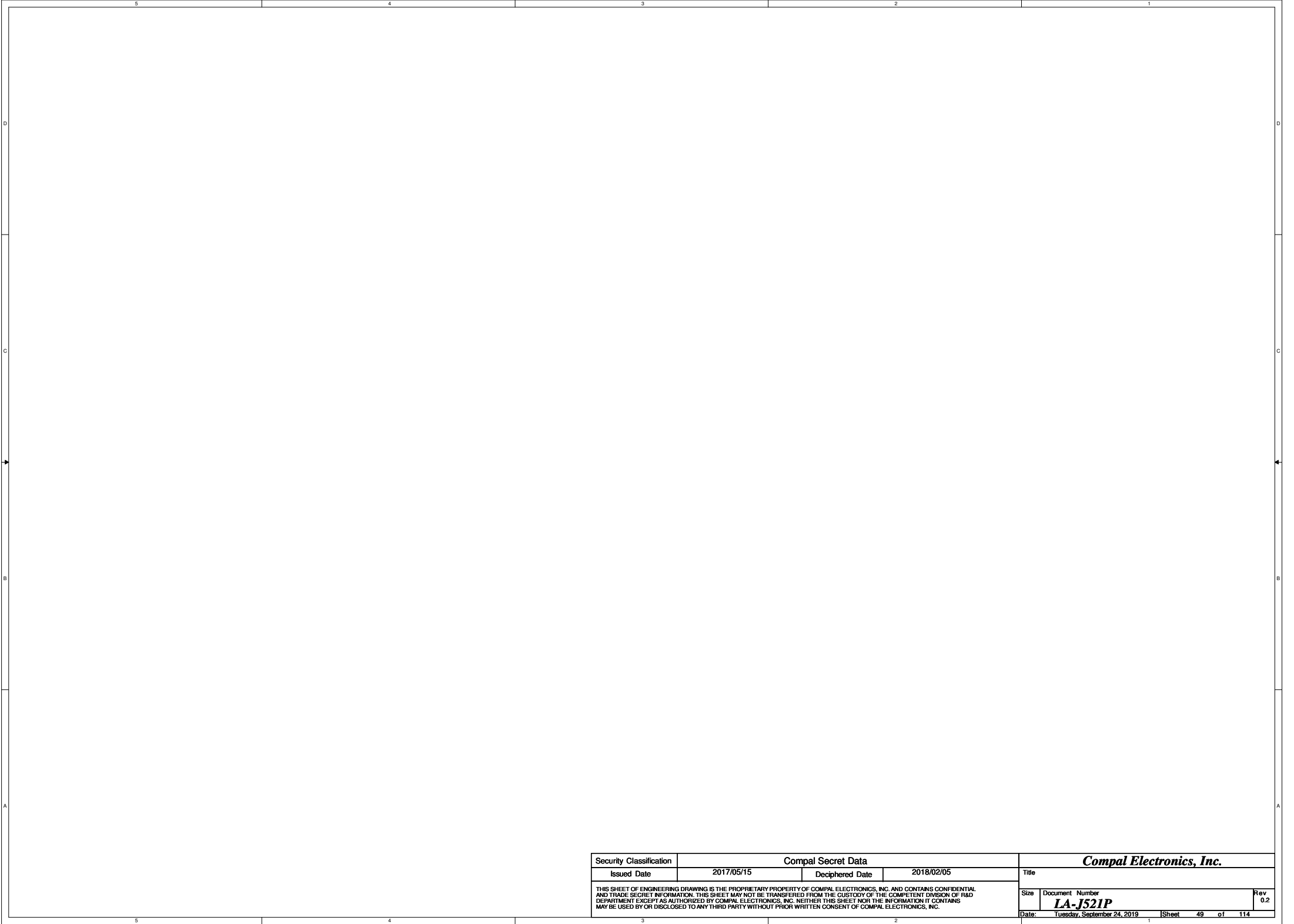
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					LA-J521P
				Rev	0.2
Date:		Tuesday, September 24, 2019		Sheet	47 of 114



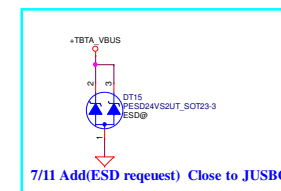
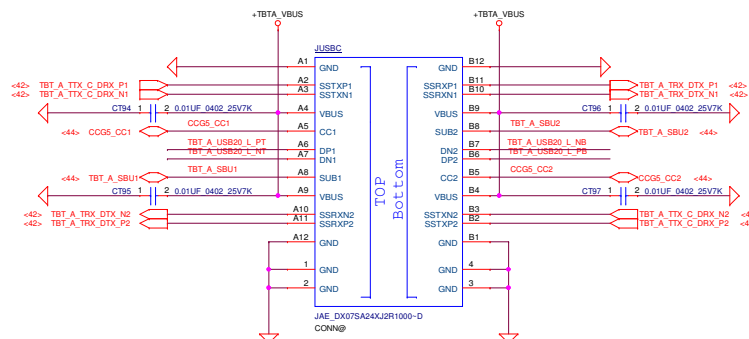
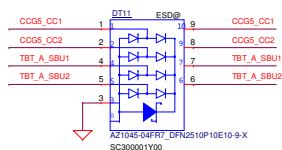
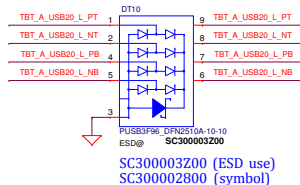
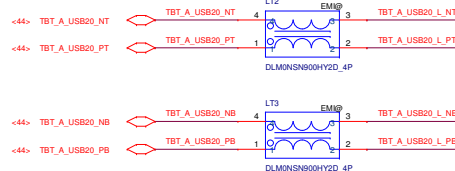
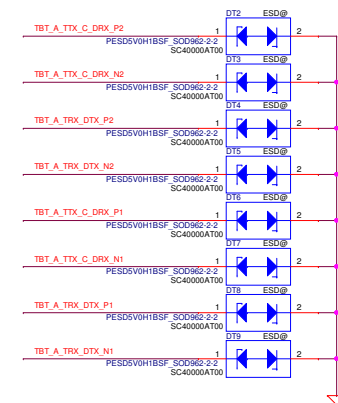
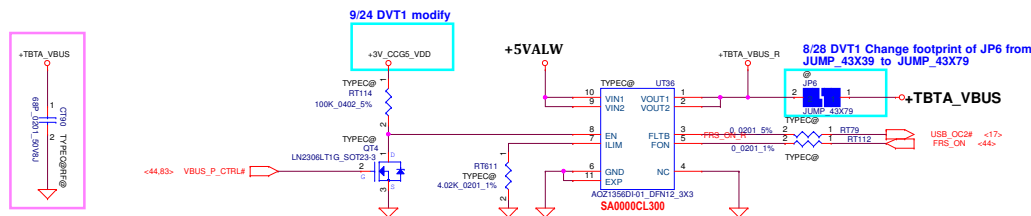
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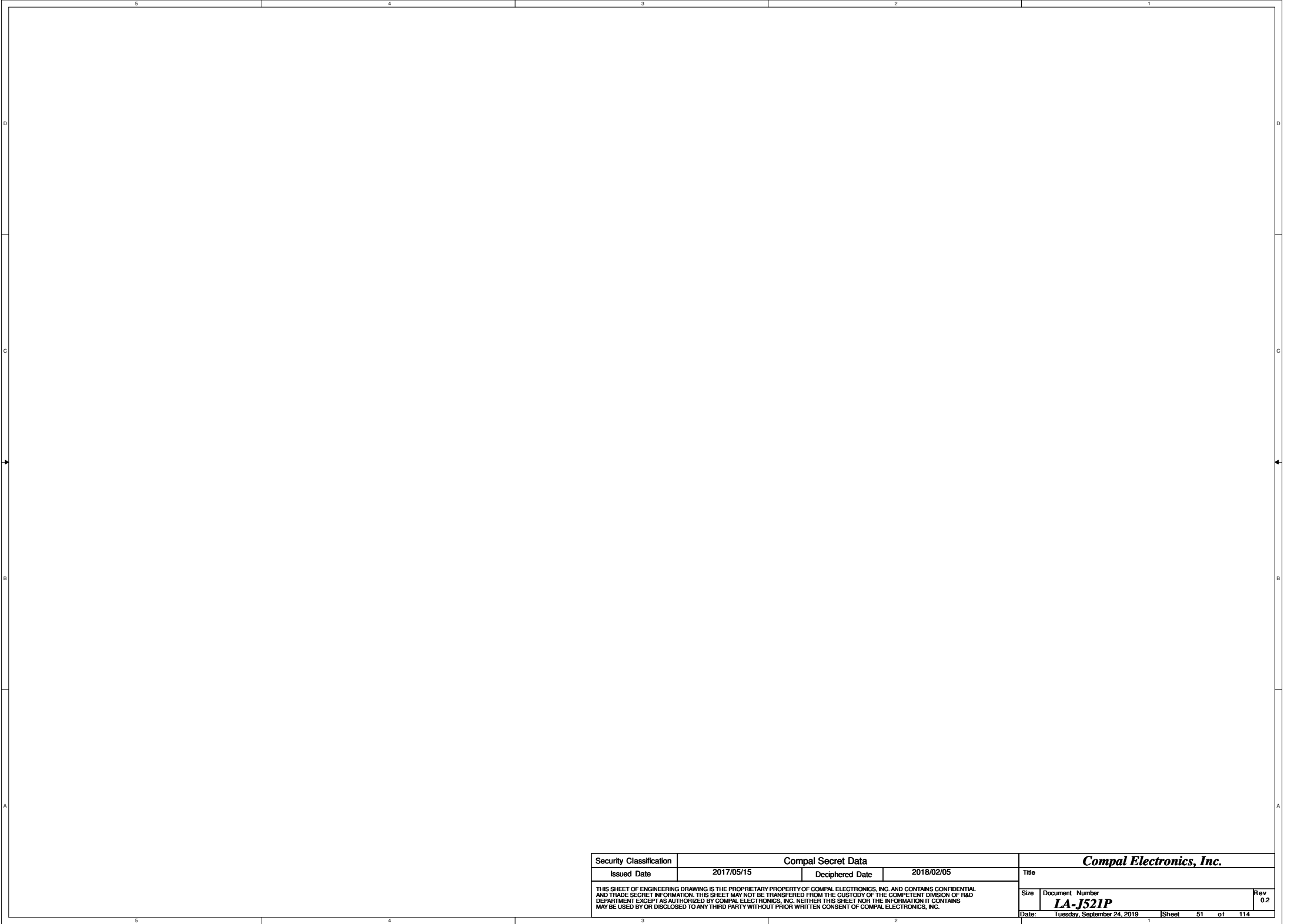
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CCG5 Power path Port1

Type-C 5V Provide Path Control
Support PD3.0
5V@3A

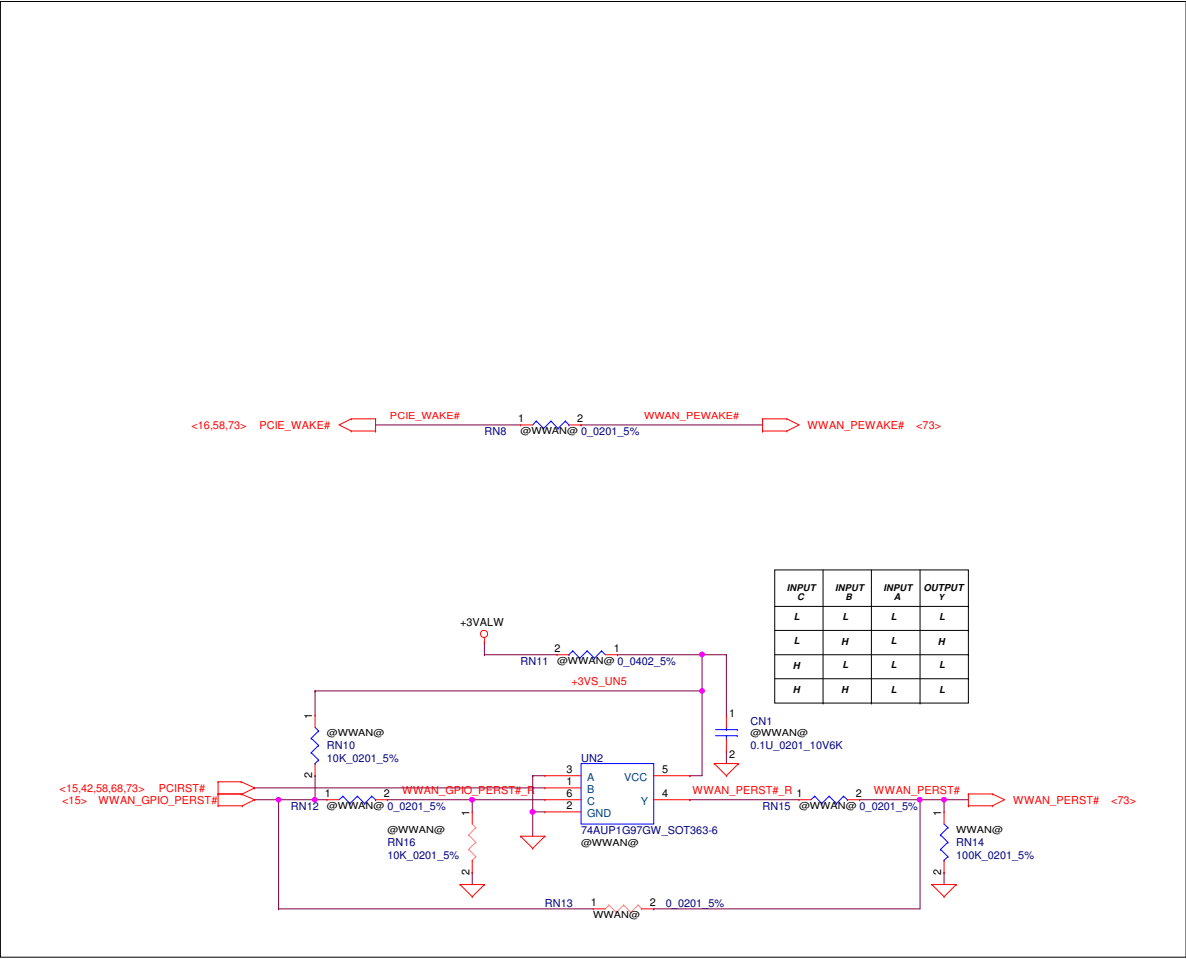


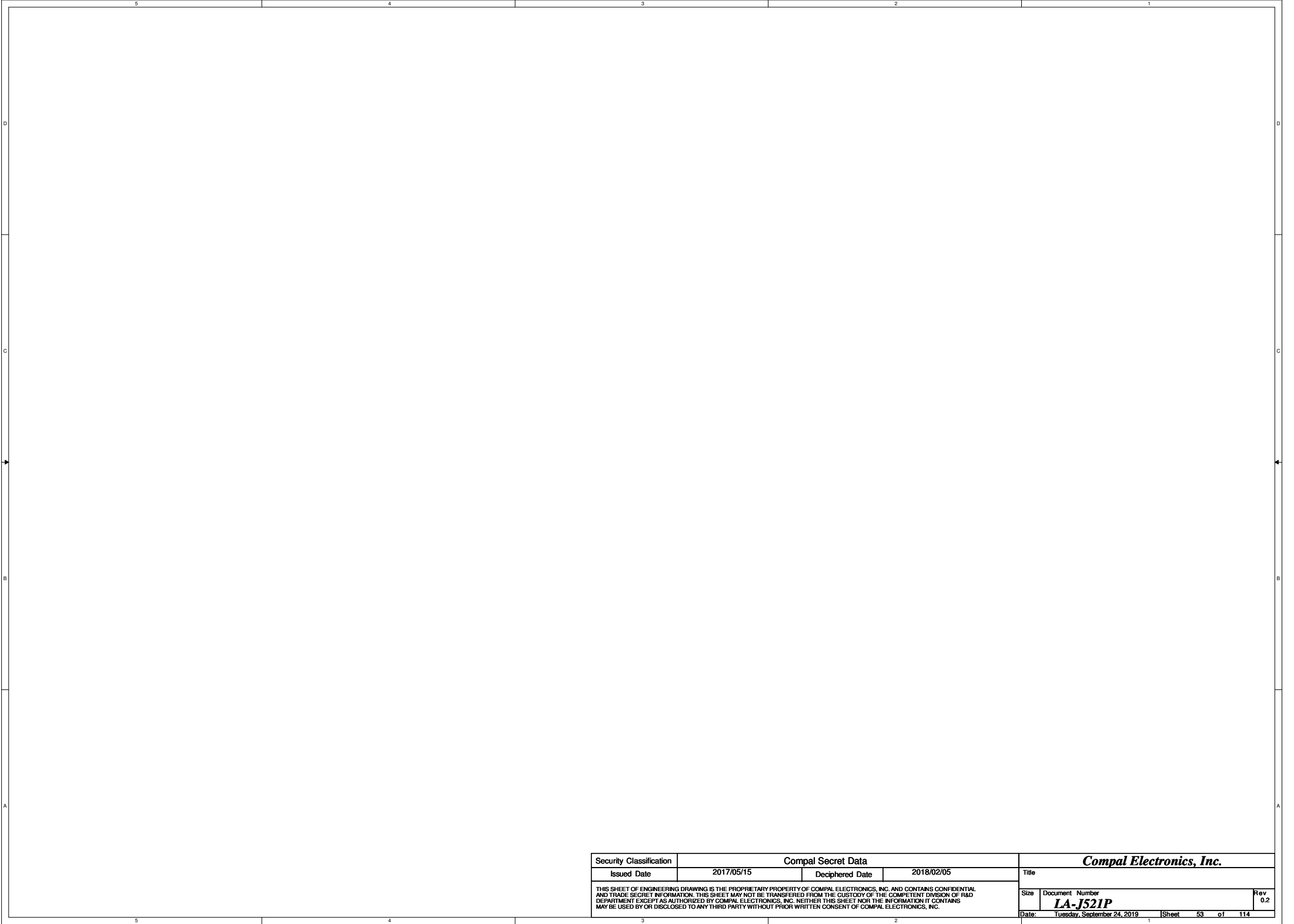
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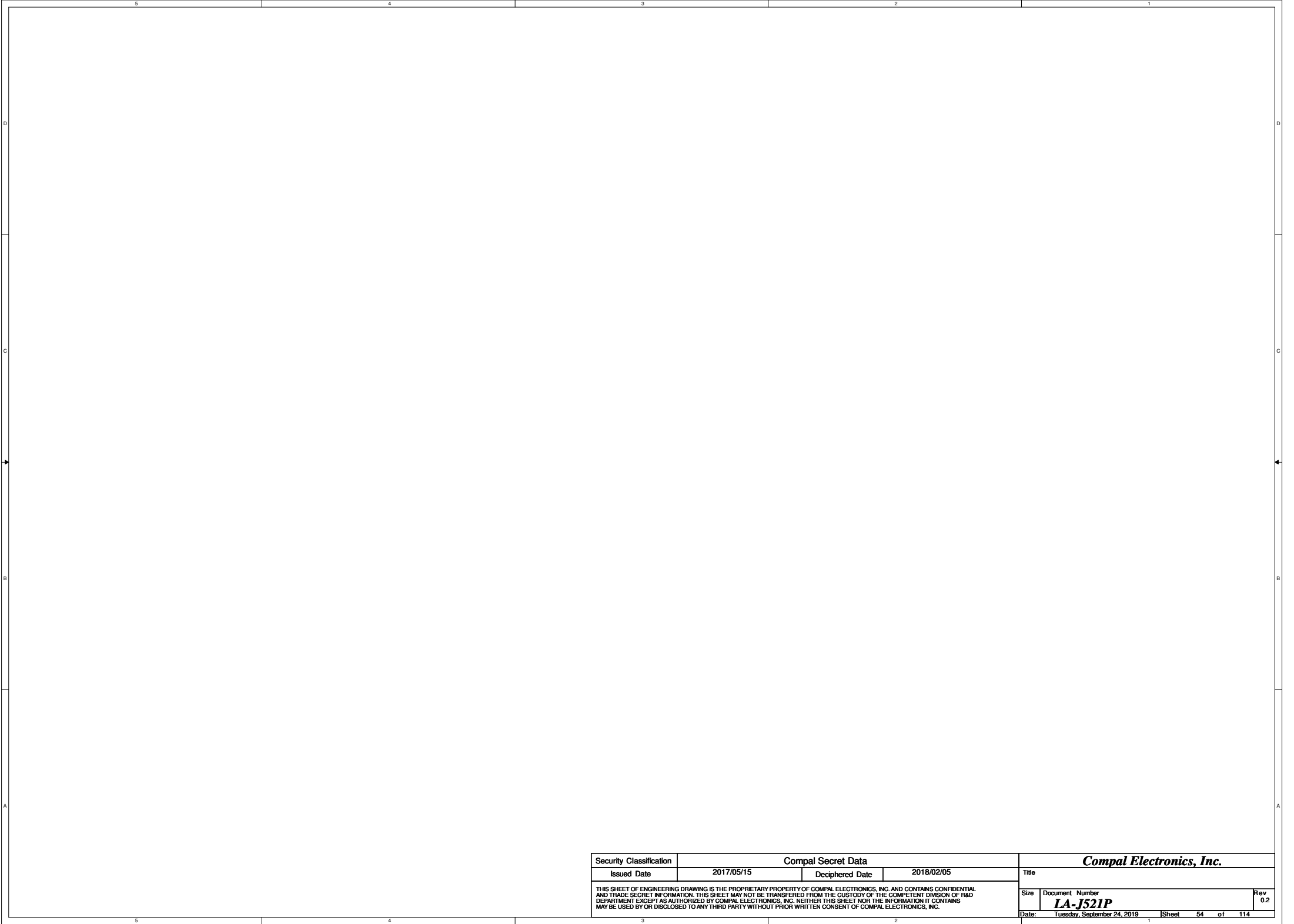
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Main Func = WWAN

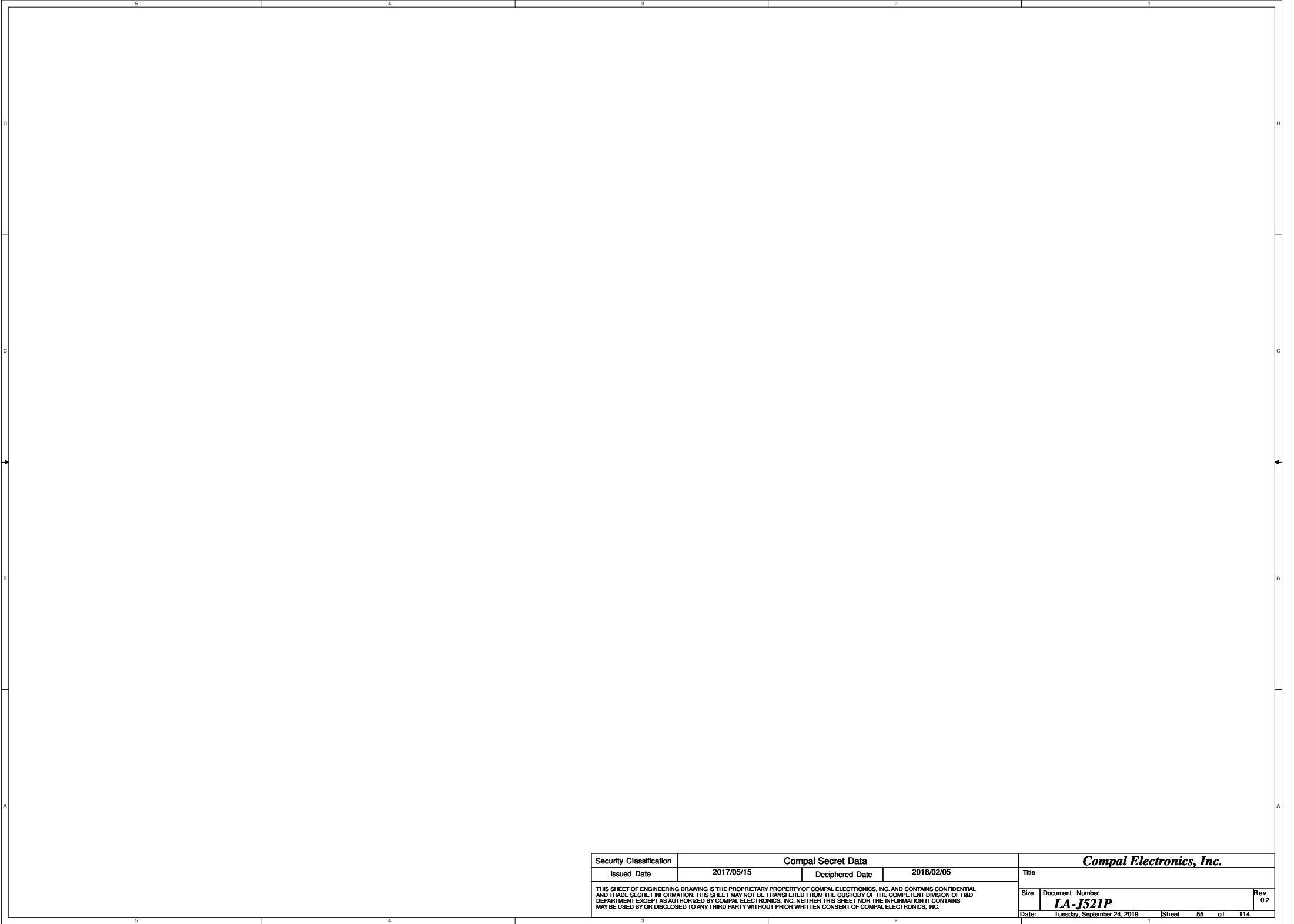




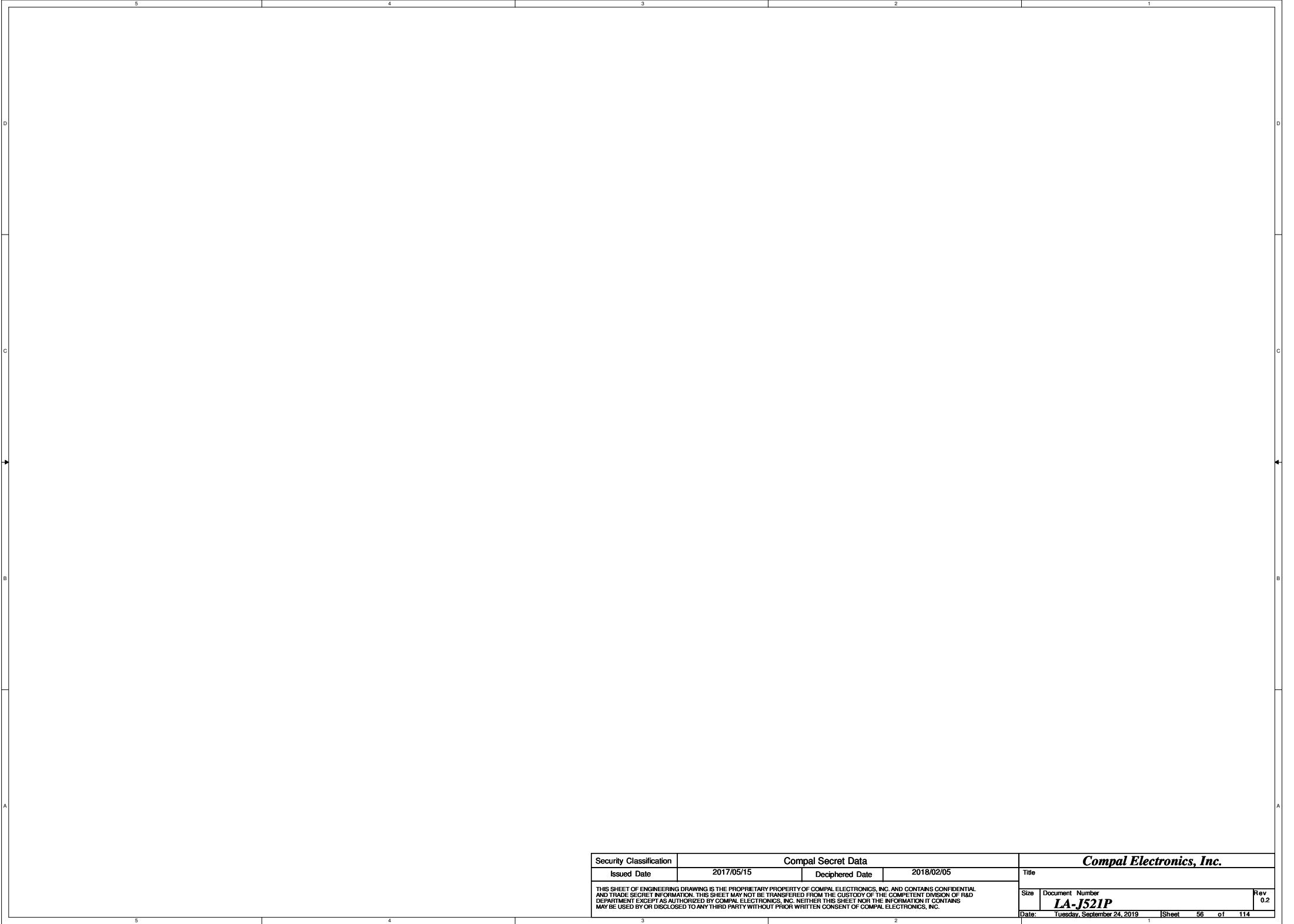
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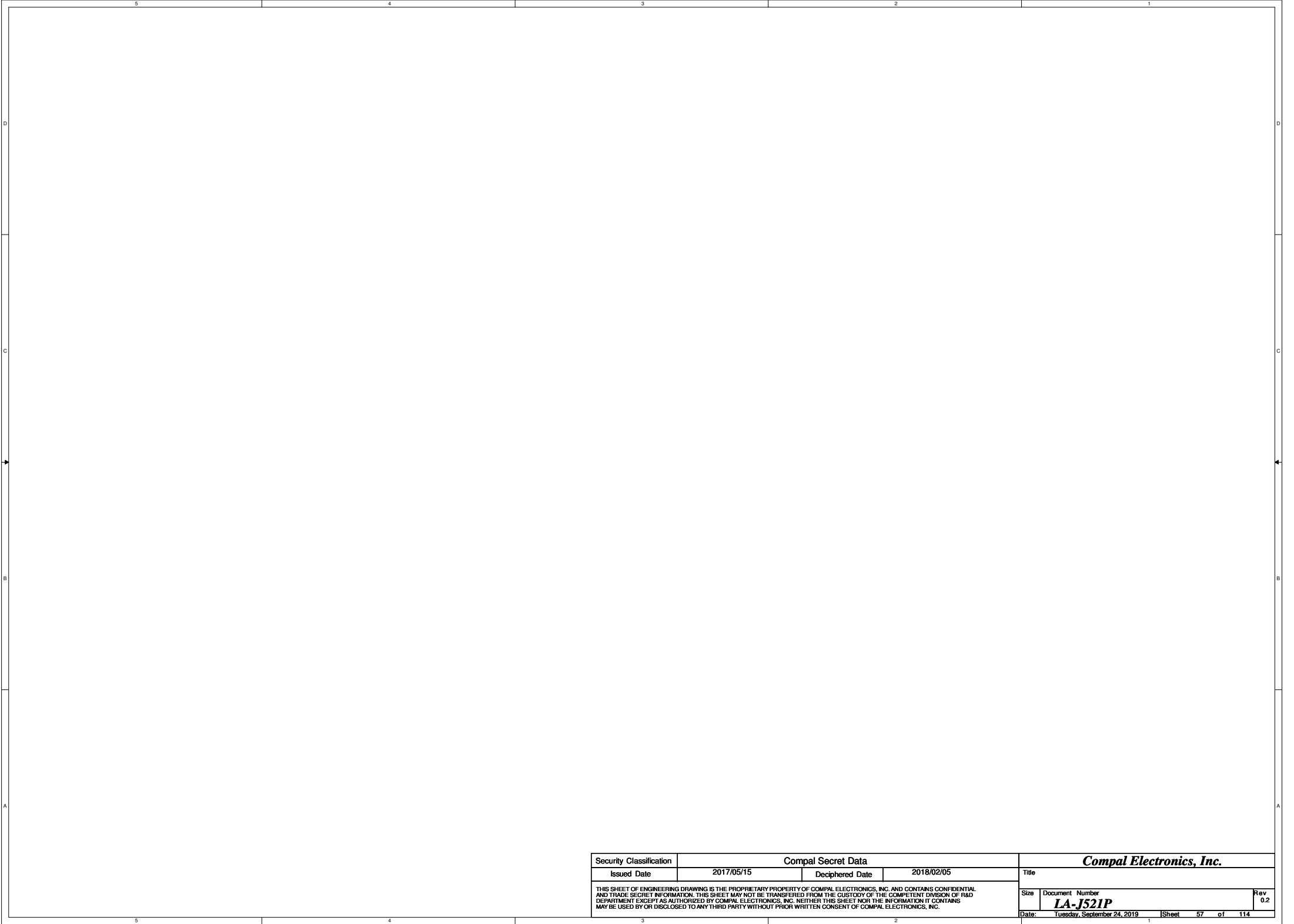
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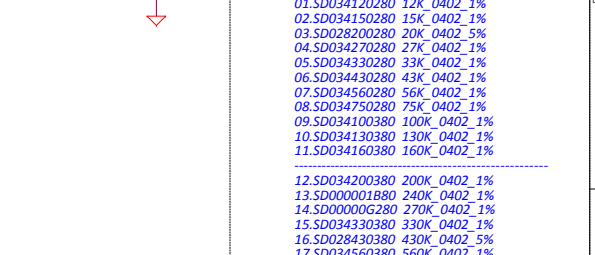
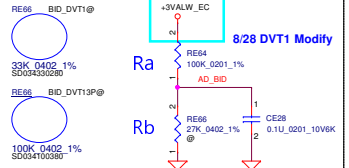
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					LA-J521P
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Date: Tuesday, September 24, 2019		Sheet 55 of 114			



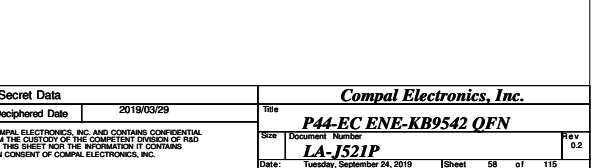
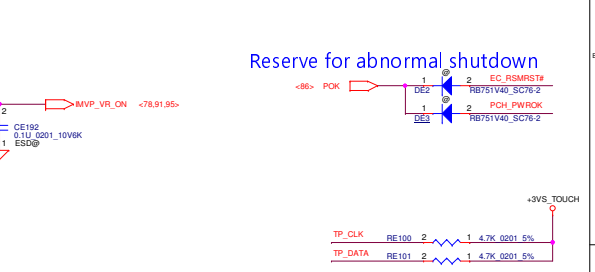
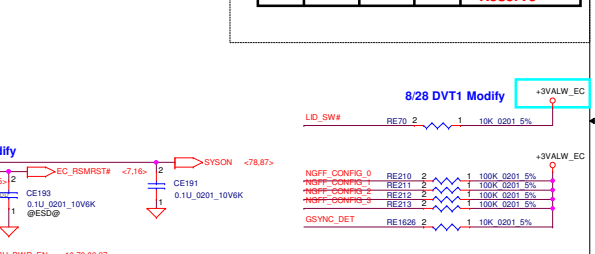
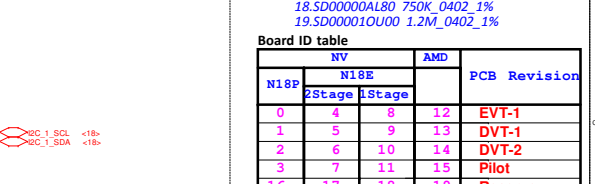
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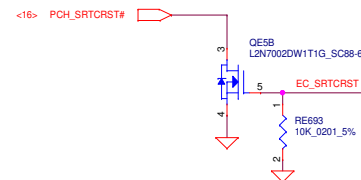
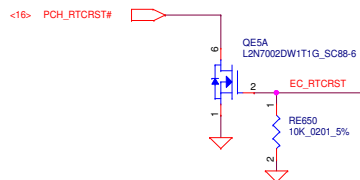
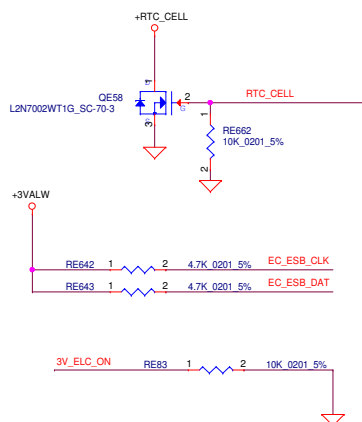
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				Date:	Tuesday, September 24, 2019
				Sheet	57 of 114
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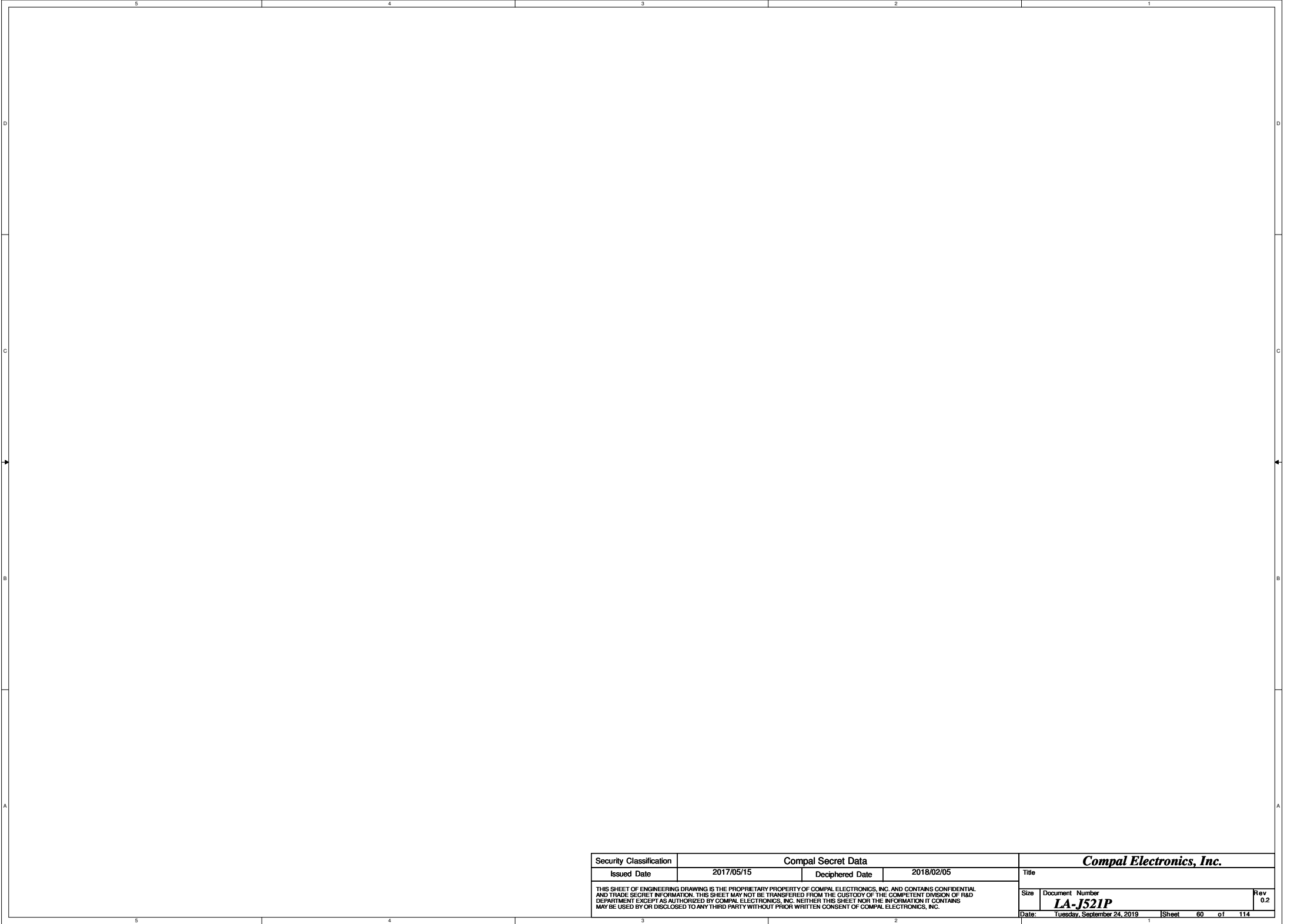
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	N18E			
	2Stage	1Stage		
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1	5	9	13	DVT-1
2	6	10	14	DVT-2
3	7	11	15	Pilot
16	17	18	19	Reserve



Main Func = S5 Lid



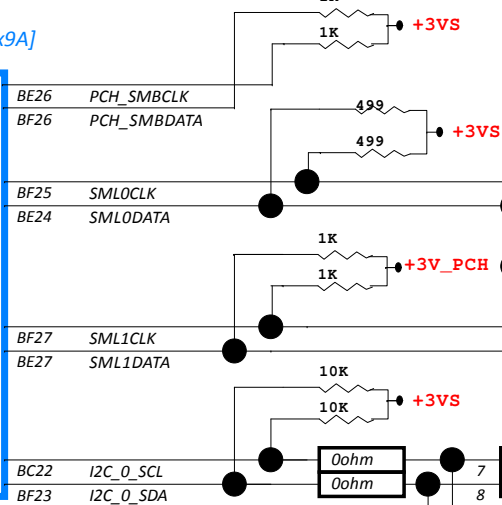
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				Rev	0.2
Date: Tuesday, September 24, 2019		Sheet		60	of 114

SMBUS Address [0x9A]

Comet Lake
PCH-H

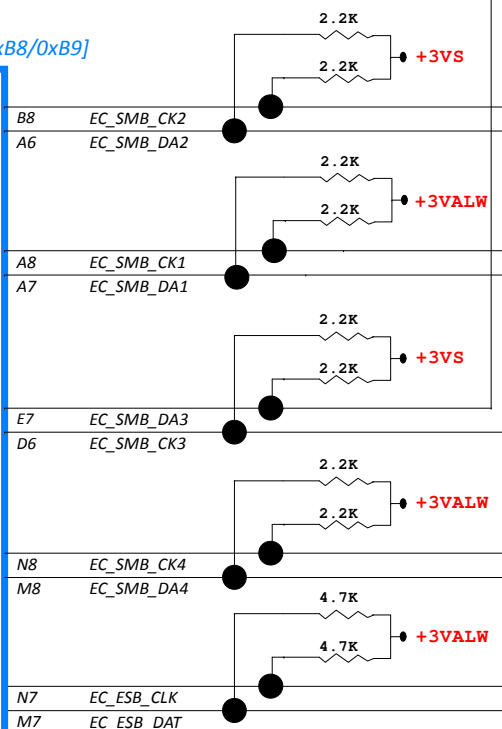


SMBUS Address [0x2C]

SMBUS Address [0x2C]

SMBUS Address [0xB8/0xB9]

KBC
KB9542G-B



SMBUS Address [0x12]

SMBUS Address [0x16]

SMBUS Address [0x08]

SMBUS Address [0x00]

SMBUS Address [0xD4/D5]

SMBUS Address [0x66/67]

SMBUS Address [0xD8/D9]

SMBUS Address [0x9A]

SMBUS Address [0xB2]

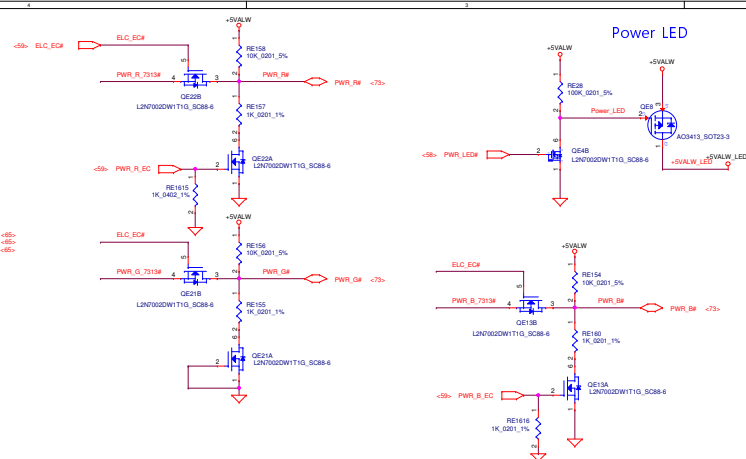
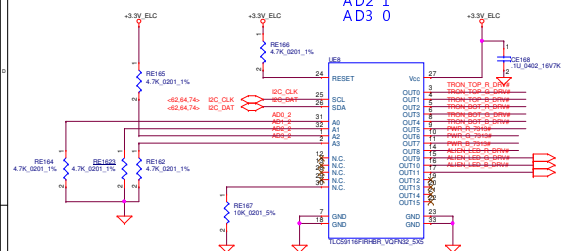
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IO3740:SMBUS Address [0xC2]

SMBUS Address [0x54]

SMBUS Address [0x9E]

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		LA-J521P		0.2	
Date:		Tuesday, September 24, 2019		Sheet	61 of 114

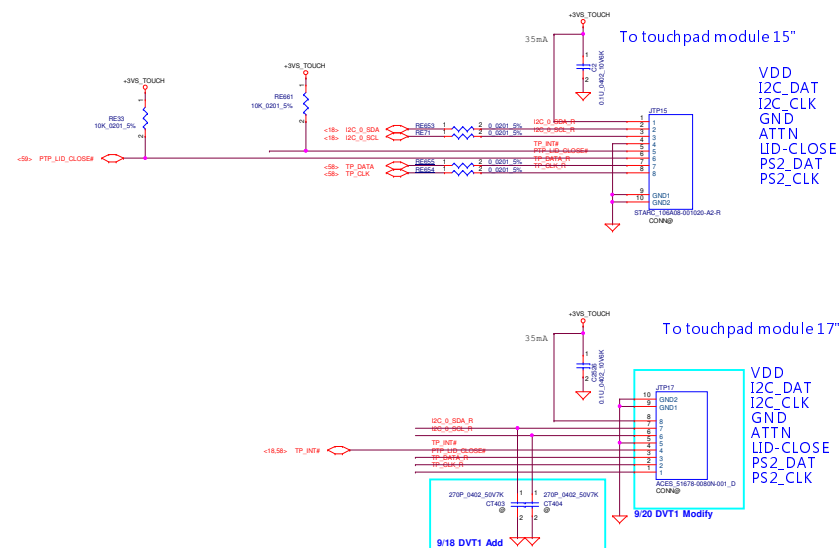
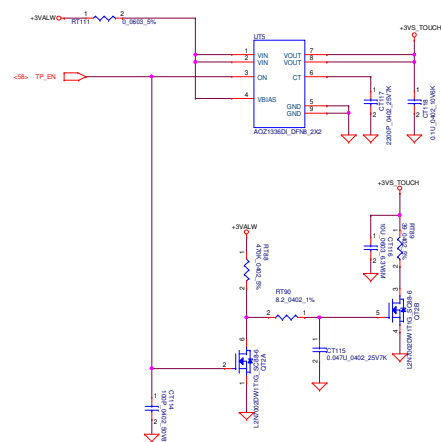

```
AD0 0
AD1 0
AD2 1
AD3 0
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Pin configuration diagram for the ACES 5000S-01-0101 (P01) module. The diagram shows a 12-pin connector with the following connections:

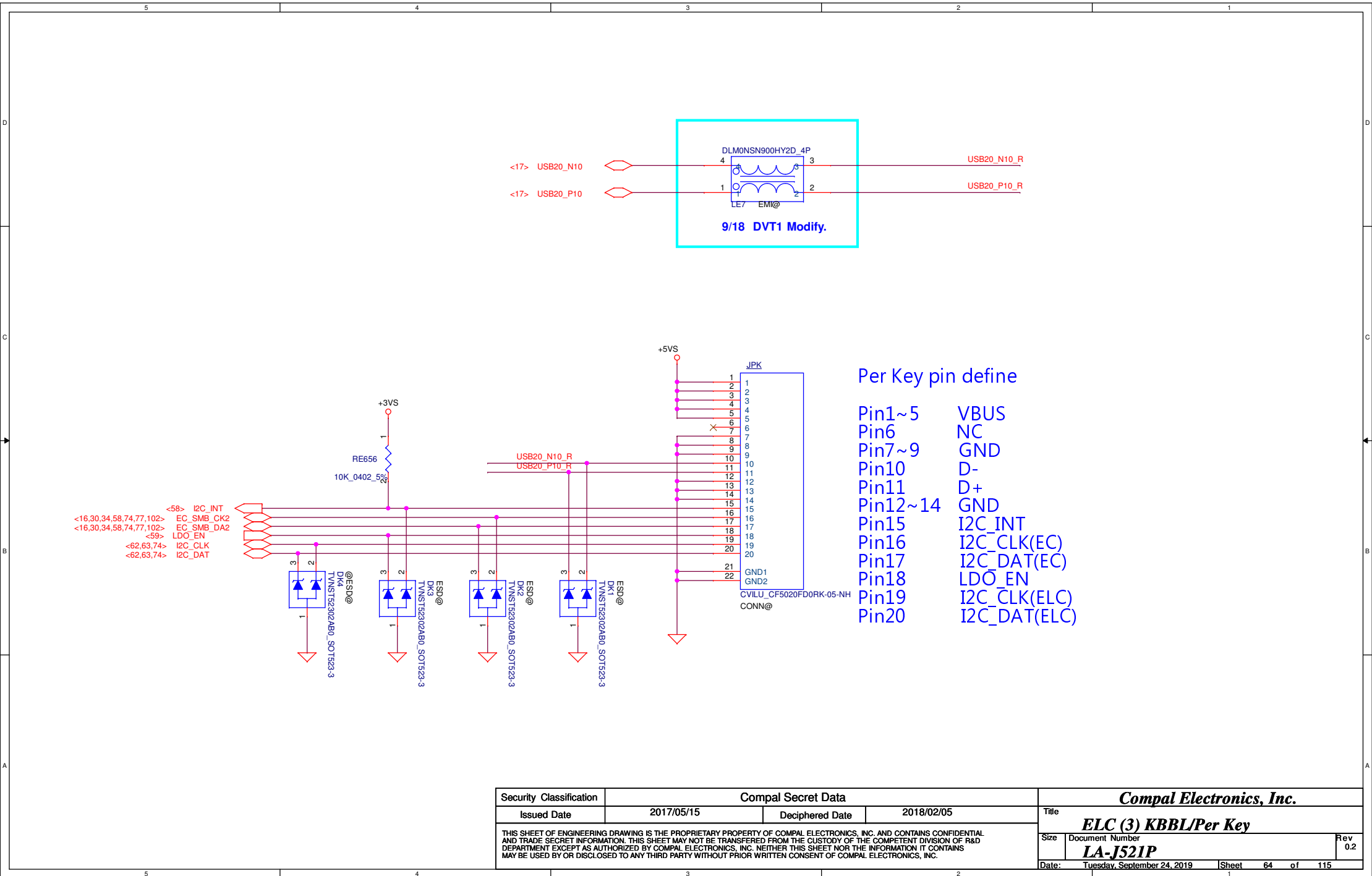
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- Pin 2: RETN
- Pin 3: TRIGL
- Pin 4: TRIGR
- Pin 5: TRIGL
- Pin 6: TRIGR
- Pin 7: TRIGL
- Pin 8: TRIGR
- Pin 9: TRIGL
- Pin 10: TRIGR
- Pin 11: TRIGL
- Pin 12: GND

The module is labeled "ACES 5000S-01-0101 (P01)".

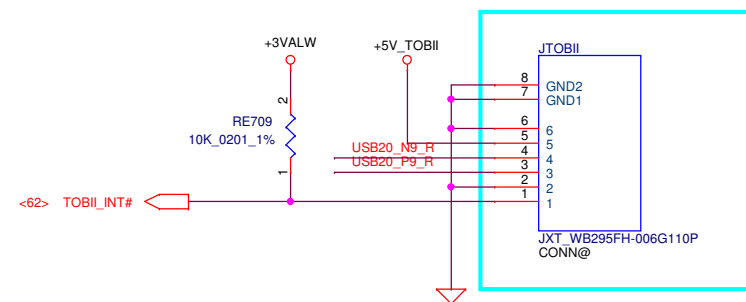
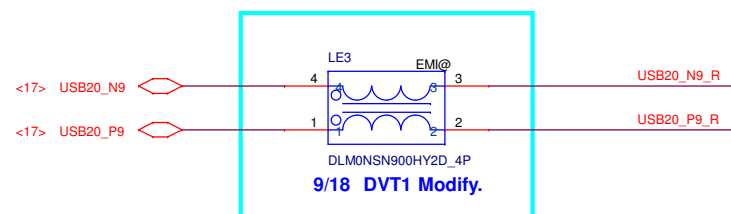
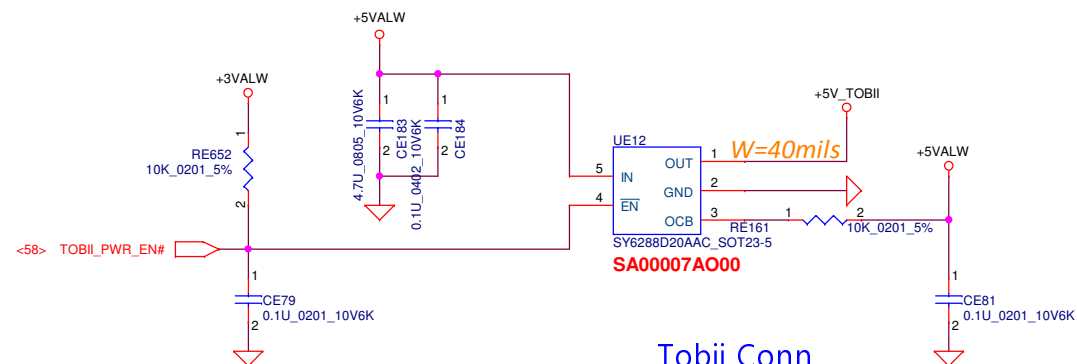
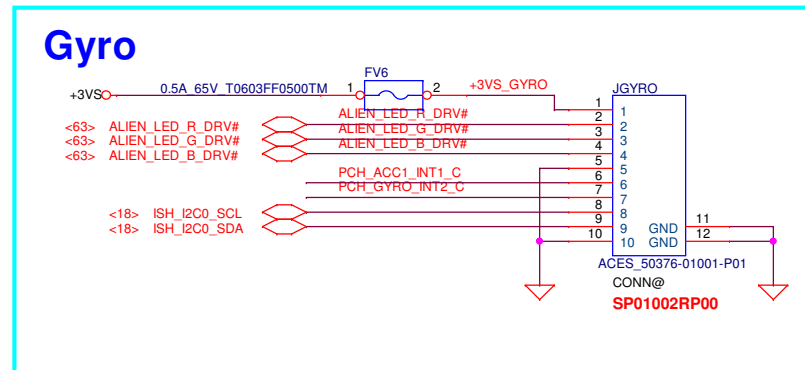
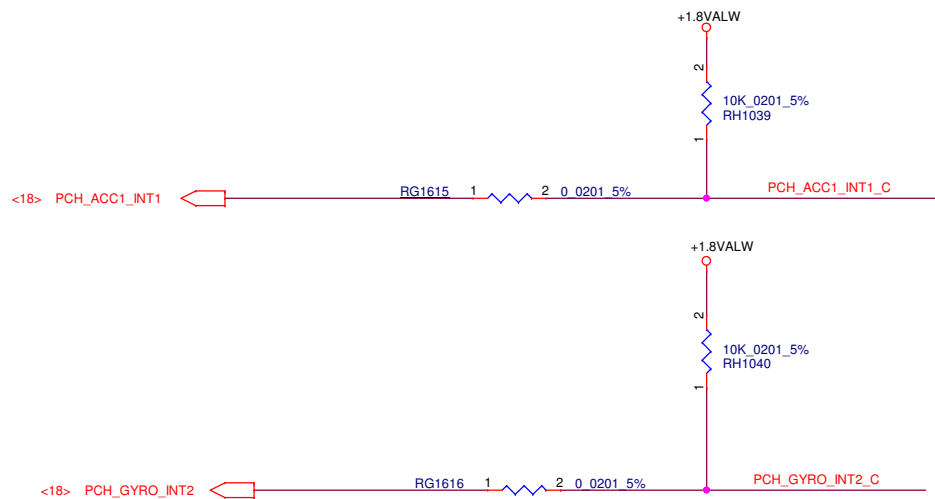


8/28 DVT1 Del Tron-Primax solution

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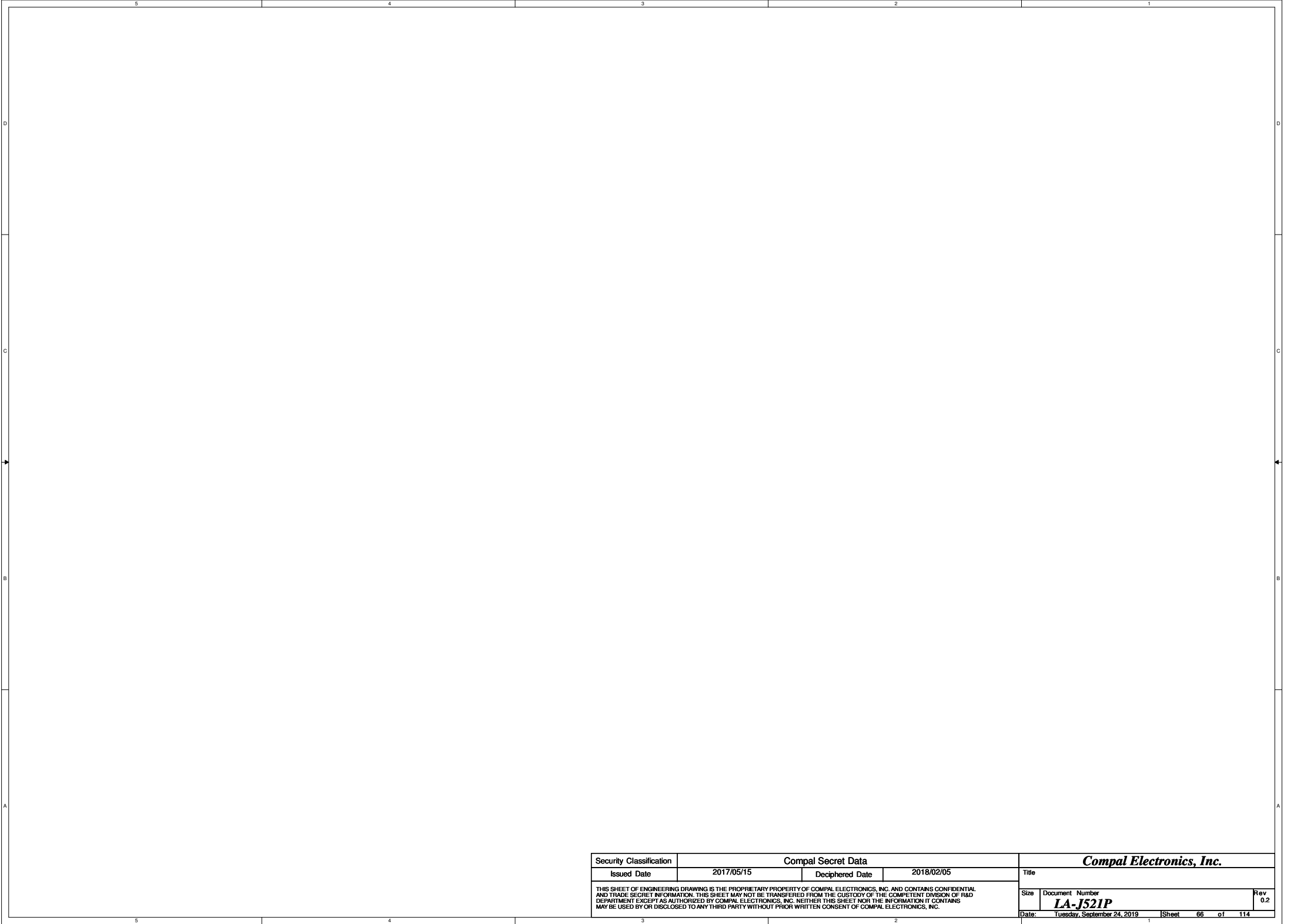


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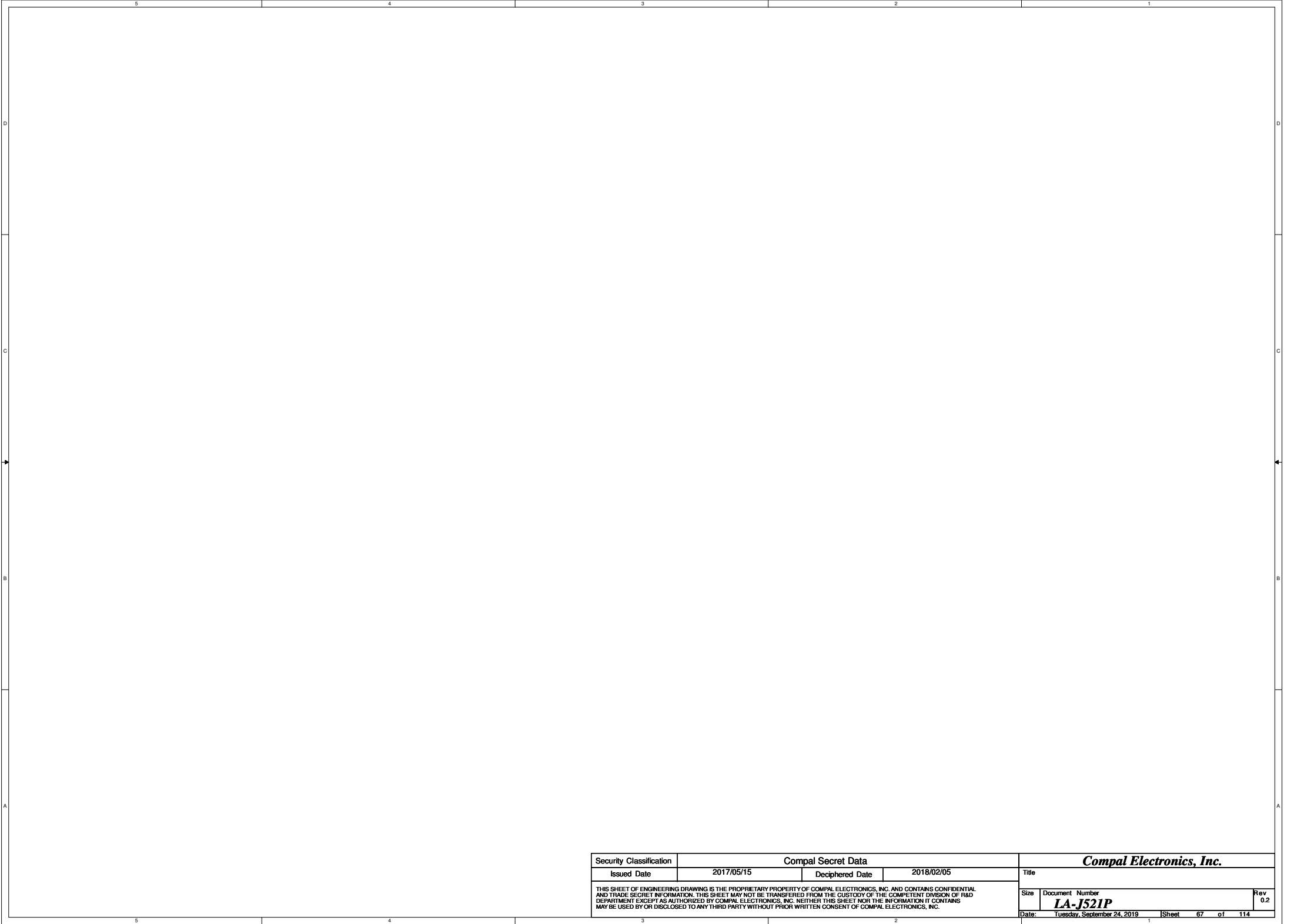


8/28 DVT1 Modify JTOBII footprint to JXT_WB295FH-006G110P_6P-T

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						Size	Document Number			Rev
						LA-J521P				0.2
Date:		Tuesday, September 24, 2019		Sheet	65	of	115			

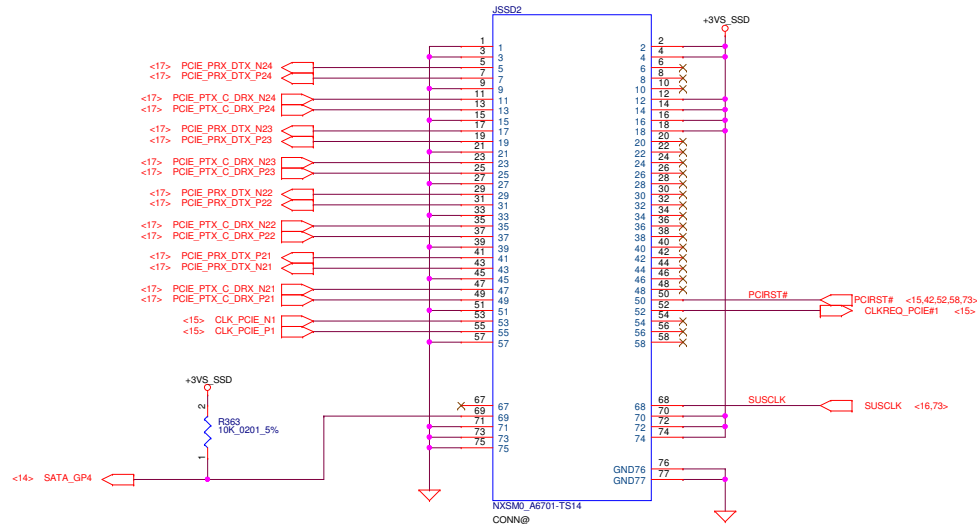


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											<i>LA-J521P</i>			0.2	
								Date: Tuesday, September 24, 2019							
						Sheet 66		of 114							

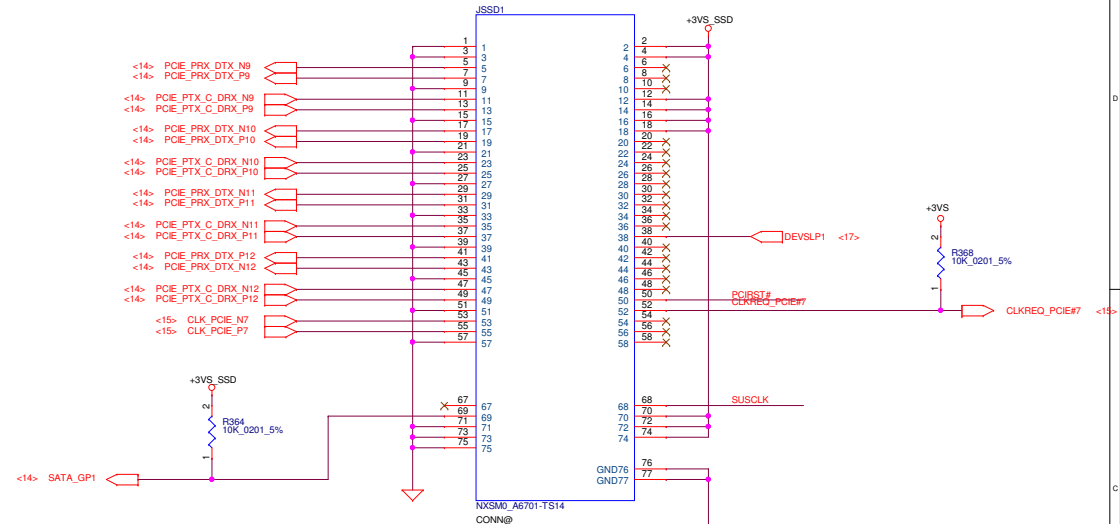


Security Classification		Compal Secret Data			<i>Compal Electronics, Inc.</i>						
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							LA-J521P	0.2			
						Date: Tuesday, September 24, 2019			Sheet 67	of 114	

PCIe SSD#2, 2280

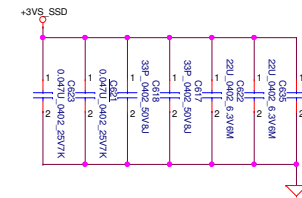


PCIe / SATA SSD SSD#1, 2280

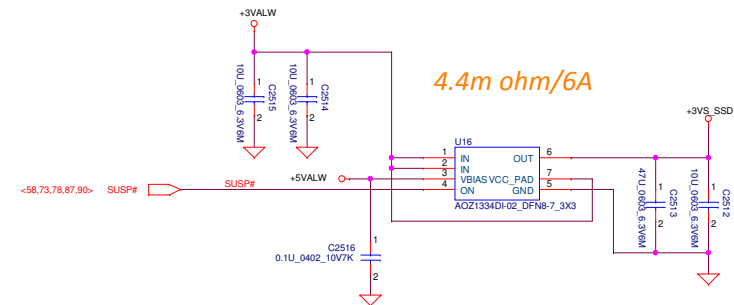
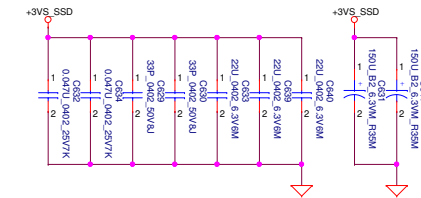


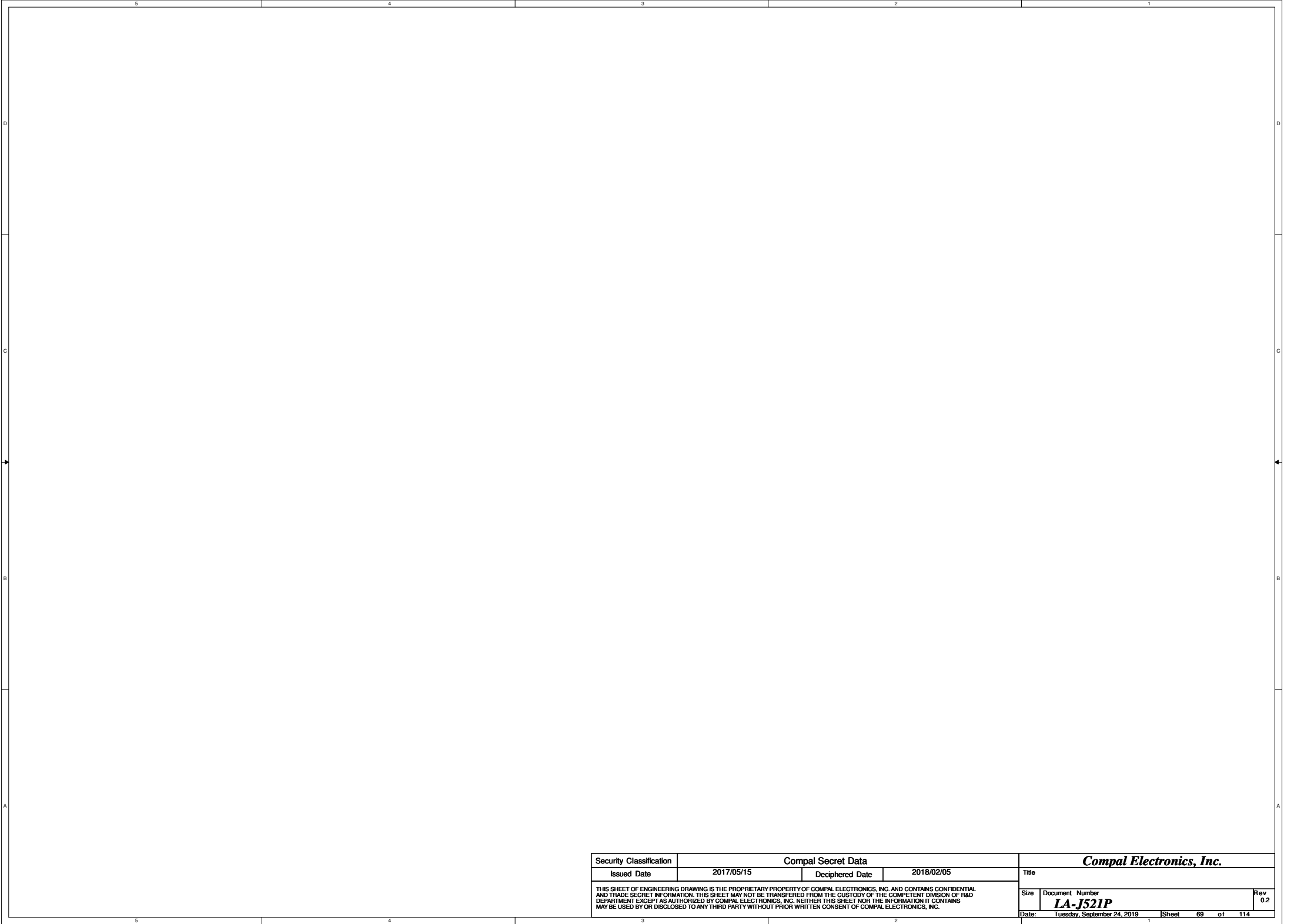
PEDET	Module Type
0	SATA
1	PCIe

JSSD2

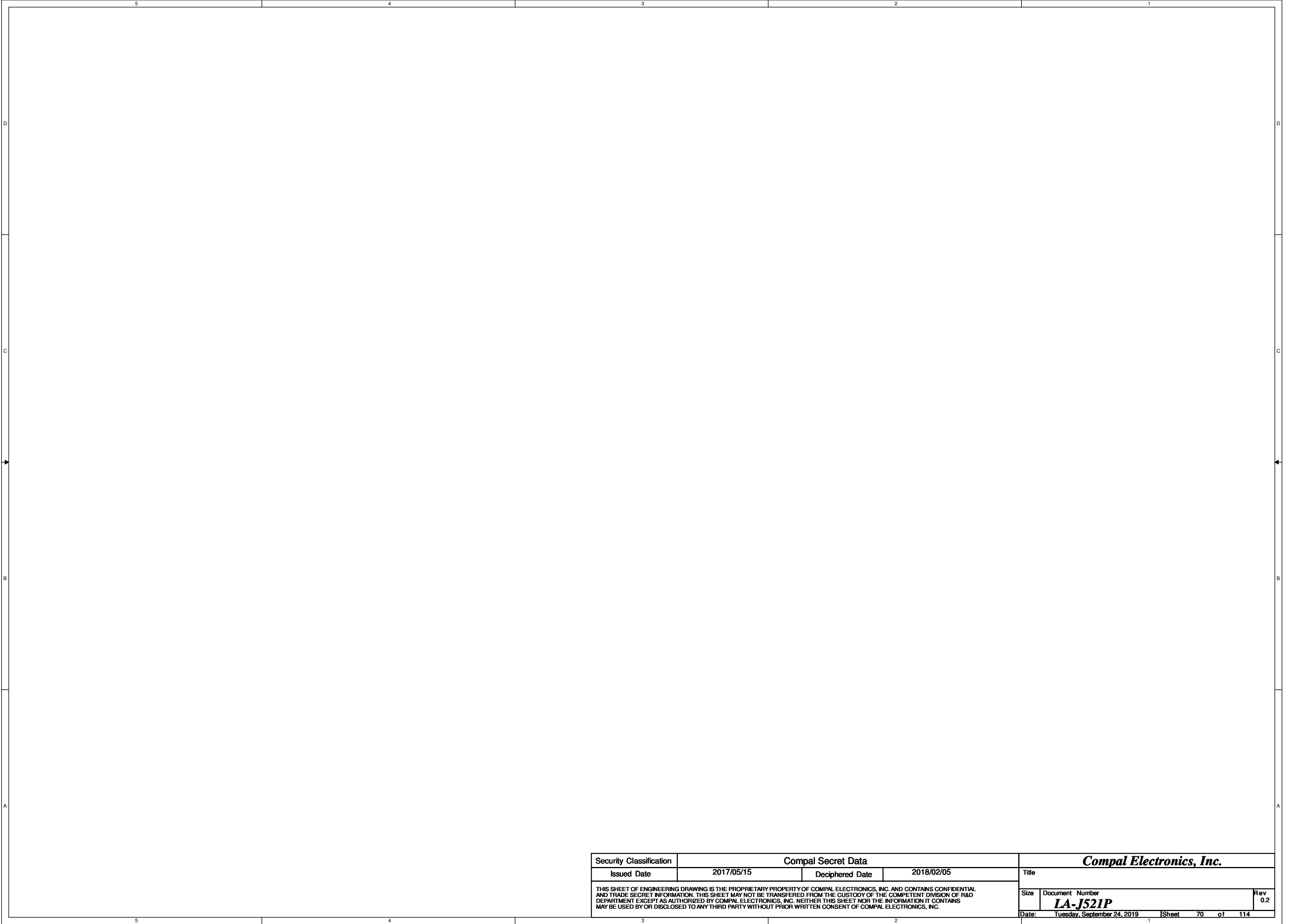


JSSD1

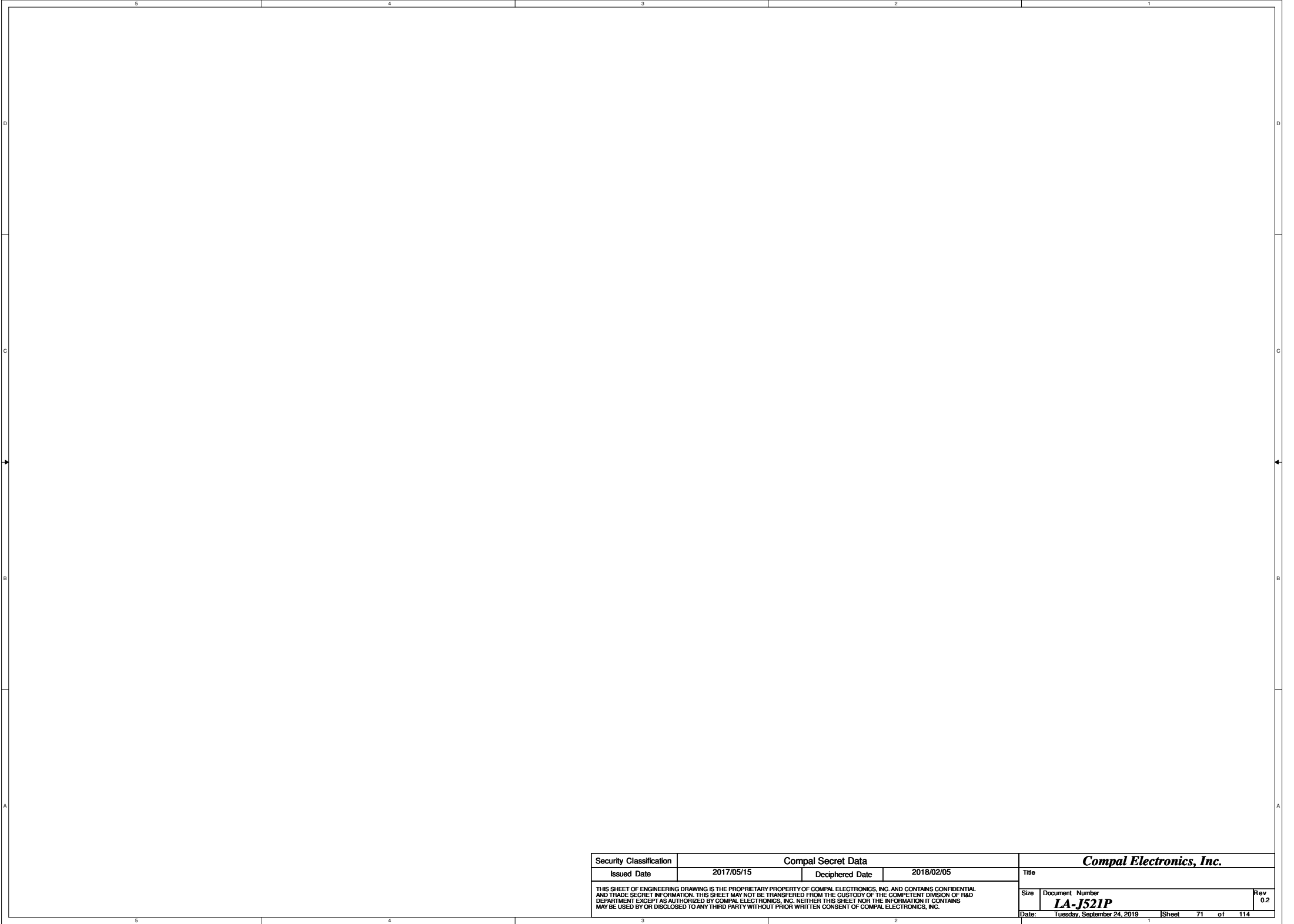




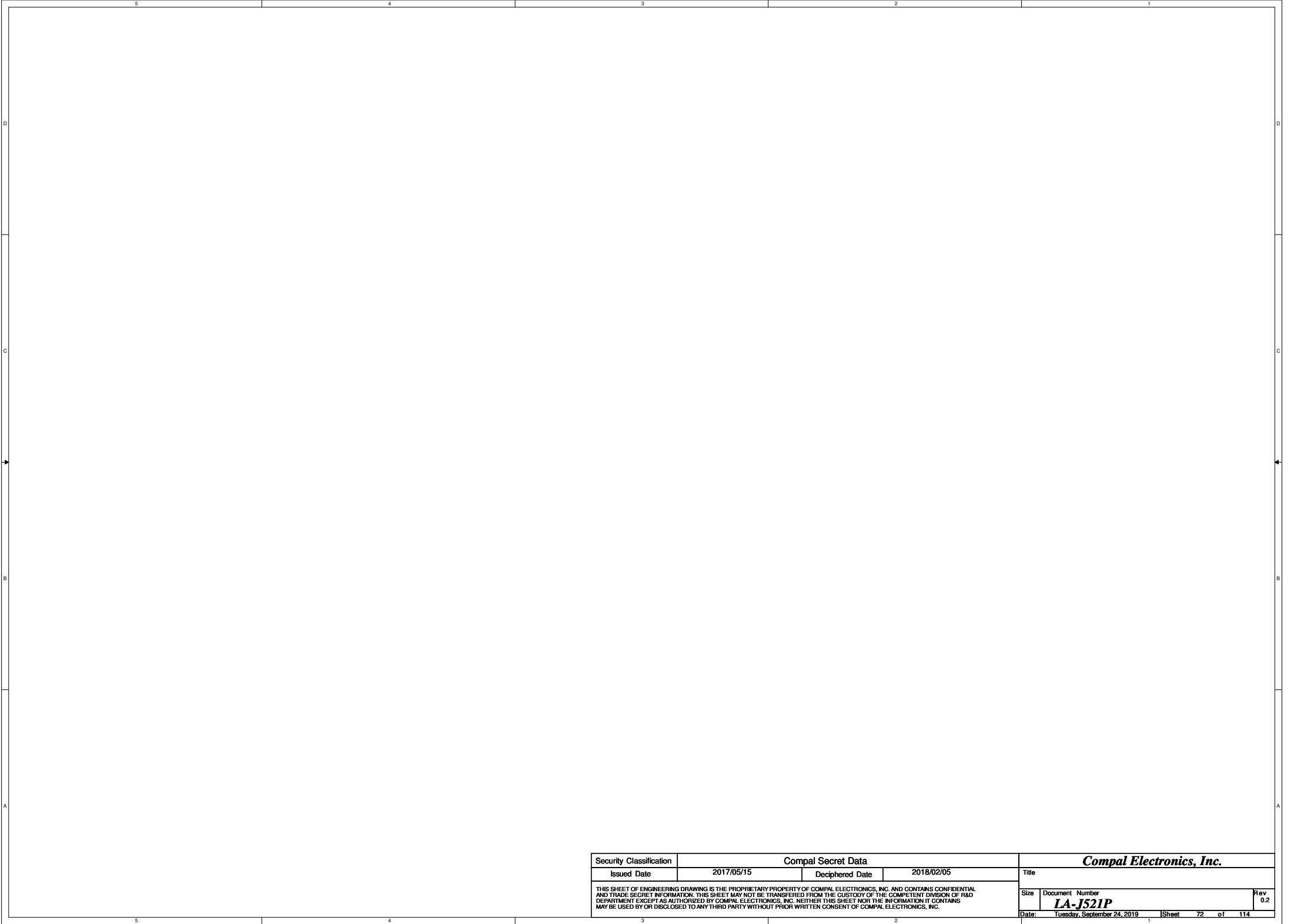
Security Classification		Compal Secret Data				<i>Compal Electronics, Inc.</i>									
Issued Date		2017/05/15		Deciphered Date		2018/02/05		Title							
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											<i>LA-J521P</i>			0.2	
								Date: Tuesday, September 24, 2019							
				Sheet		69		of 114							



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											<i>LA-J521P</i>			0.2	
								Date: Tuesday, September 24, 2019							
						Sheet 70		of 114							

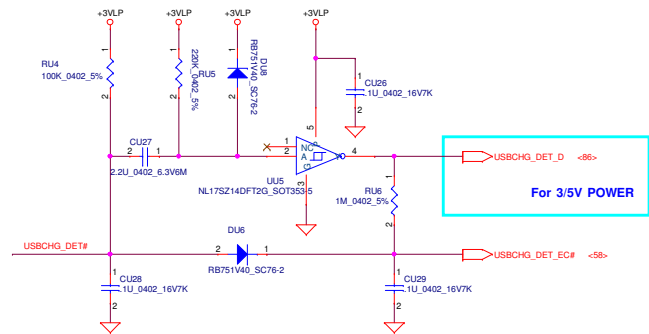


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									LA-J521P	0.2
						Date:			Tuesday, September 24, 2019	Sheet 71 of 114

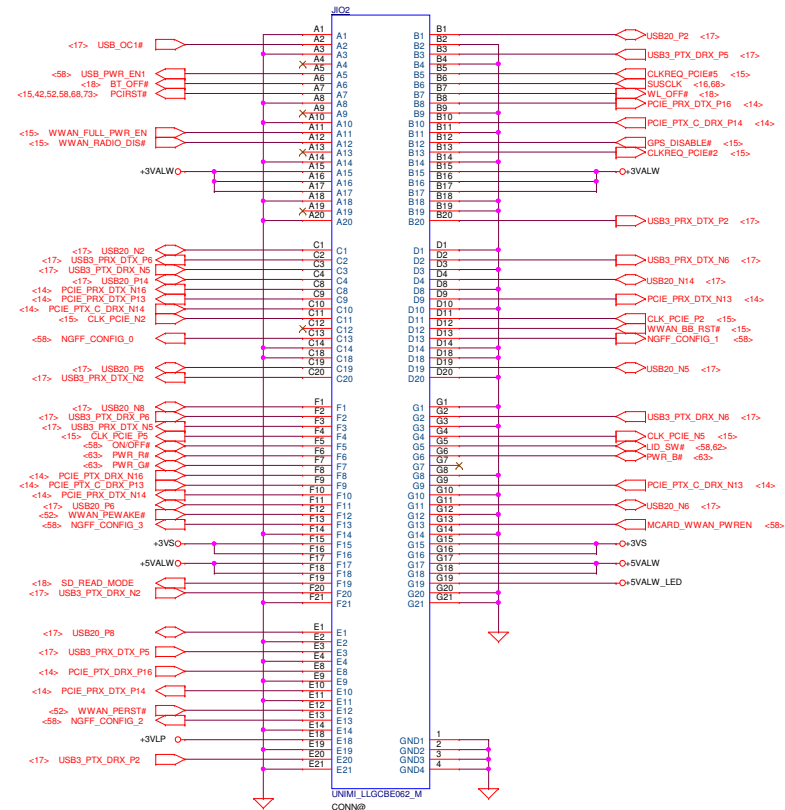


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					LA-J521P
				Rev	0.2
Date: Tuesday, September 24, 2019		Sheet 72 of 114			

USB charge for DC S5

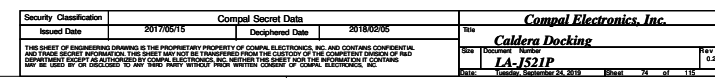
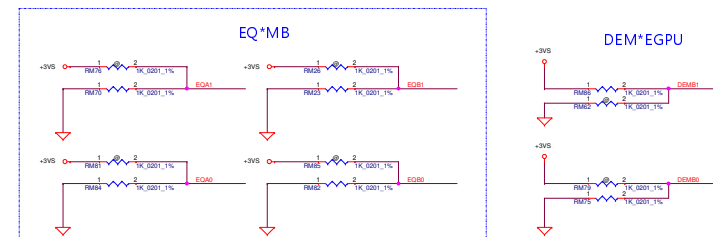
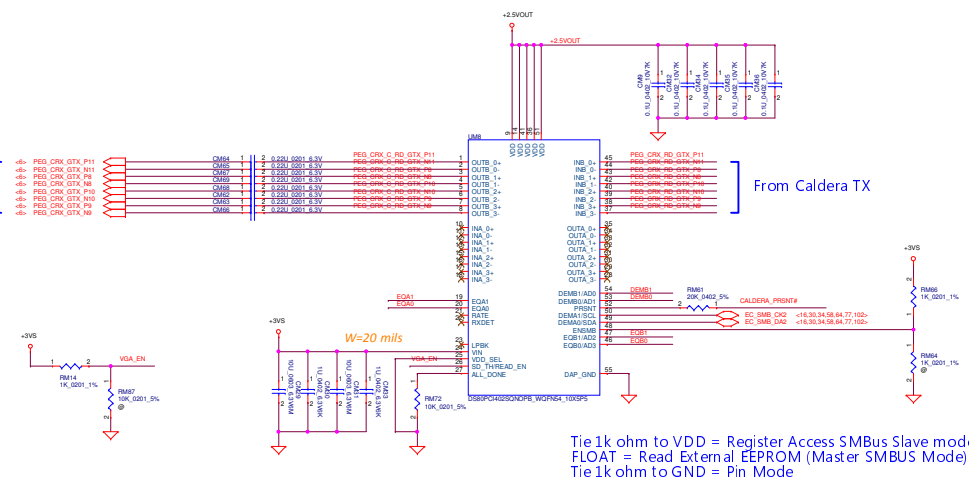
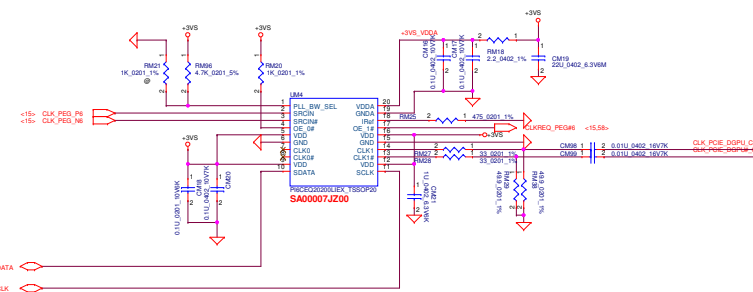
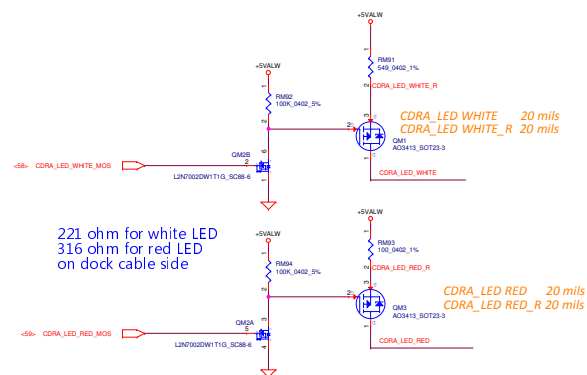
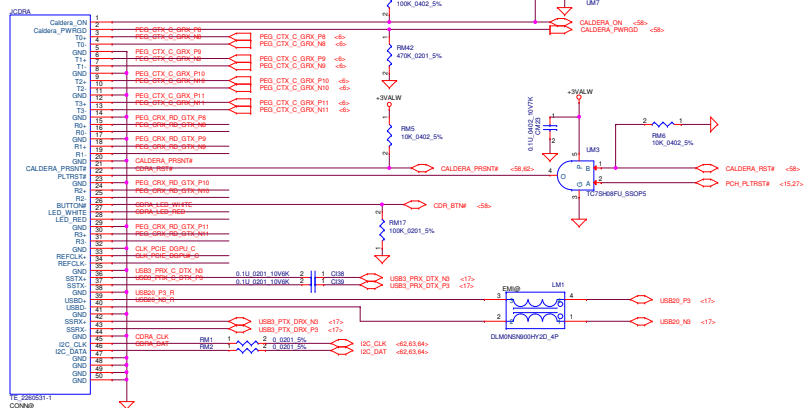


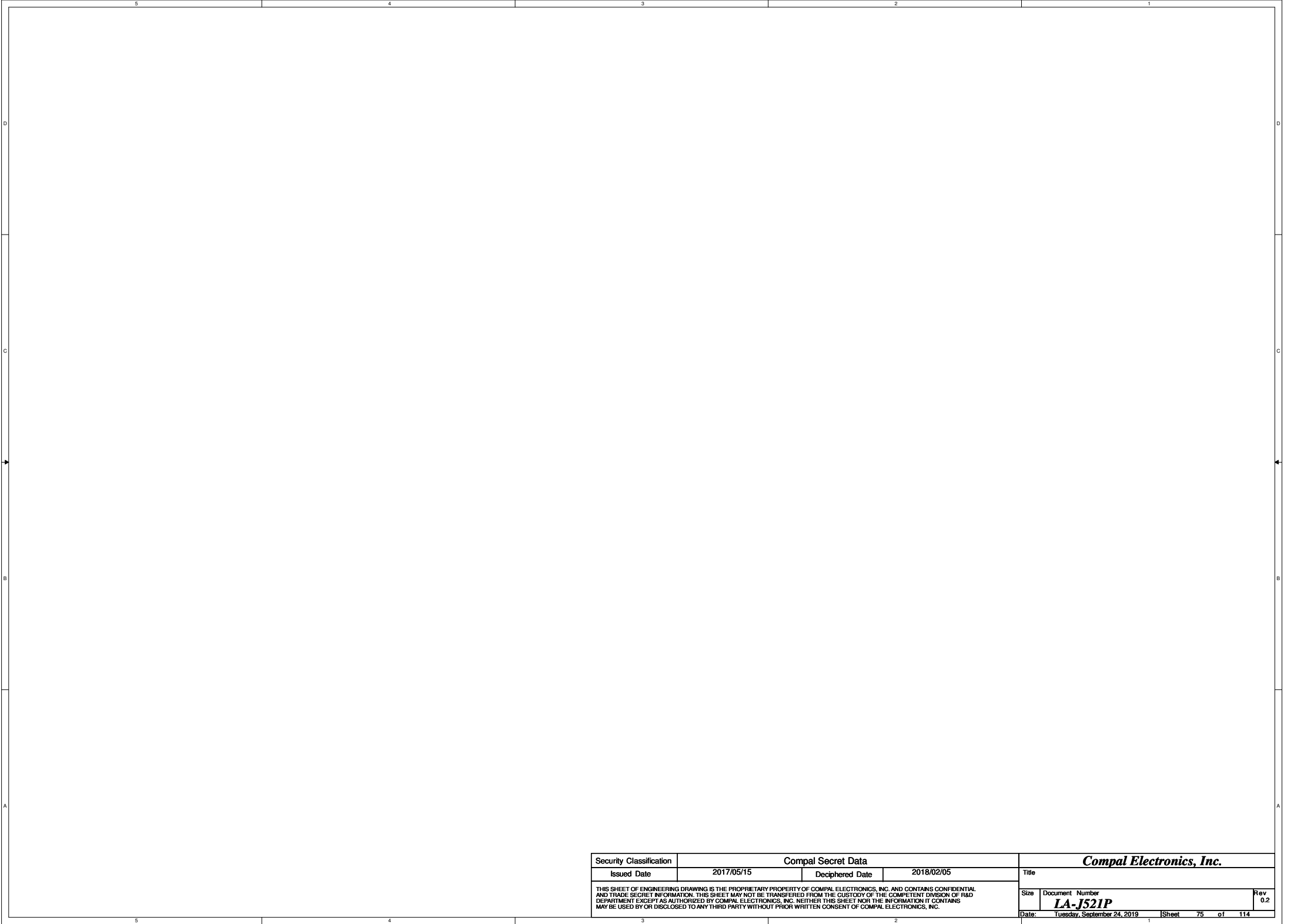
For Audio DB conn



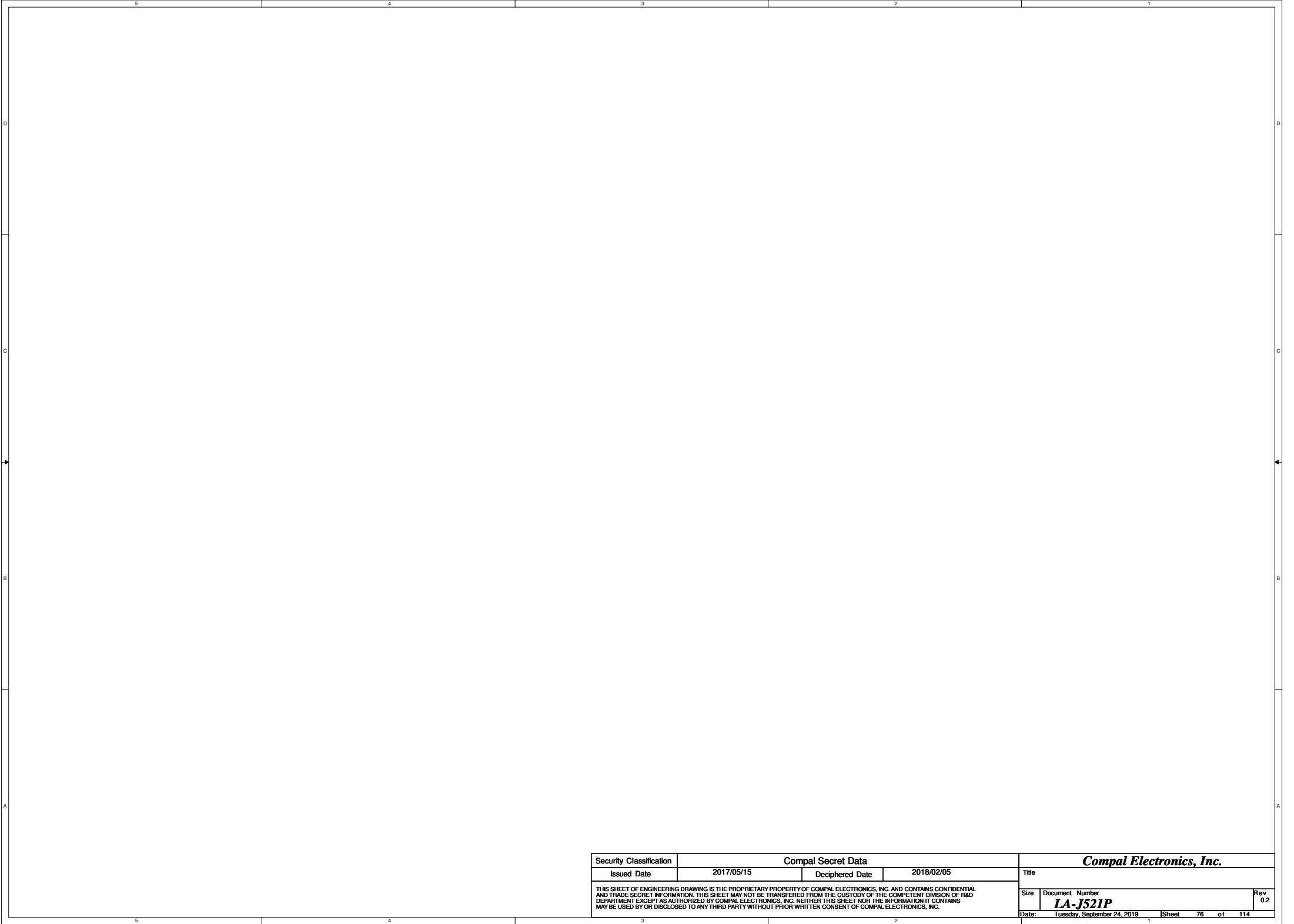
For USB DB conn

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Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title
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1A-J521P				0.2
Date: Tuesday, September 24, 2019				Sheet 73 of 115



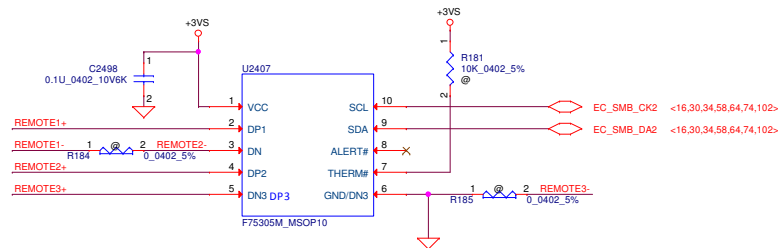


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Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title	
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					LA-J521P
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				Date:	Tuesday, September 24, 2019
				Sheet	75 of 114



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					LA-J521P
				Rev	0.2
Date: Tuesday, September 24, 2019		Sheet 76 of 114			

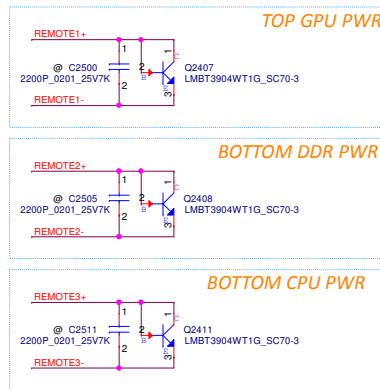
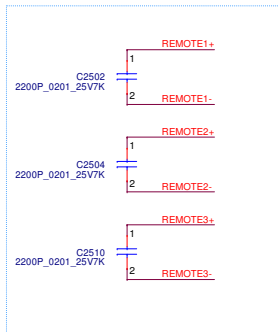
Fintek thermal sensor---> CPU core, DIMM



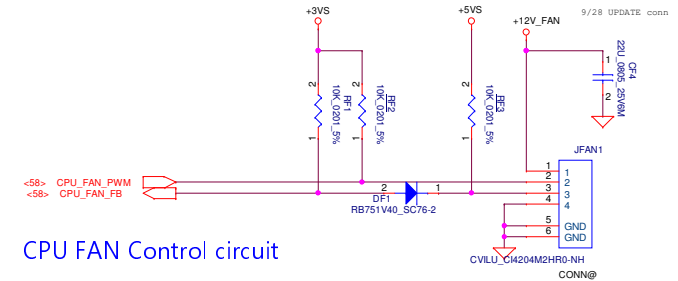
Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR

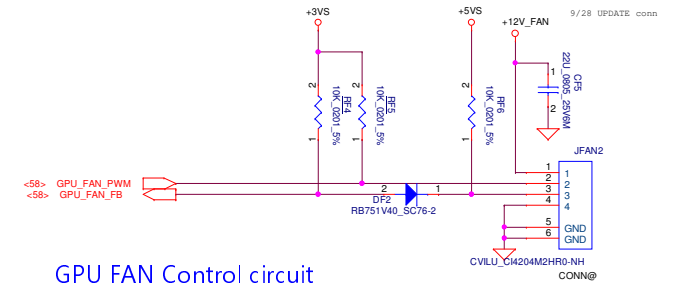
Close U2407



REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

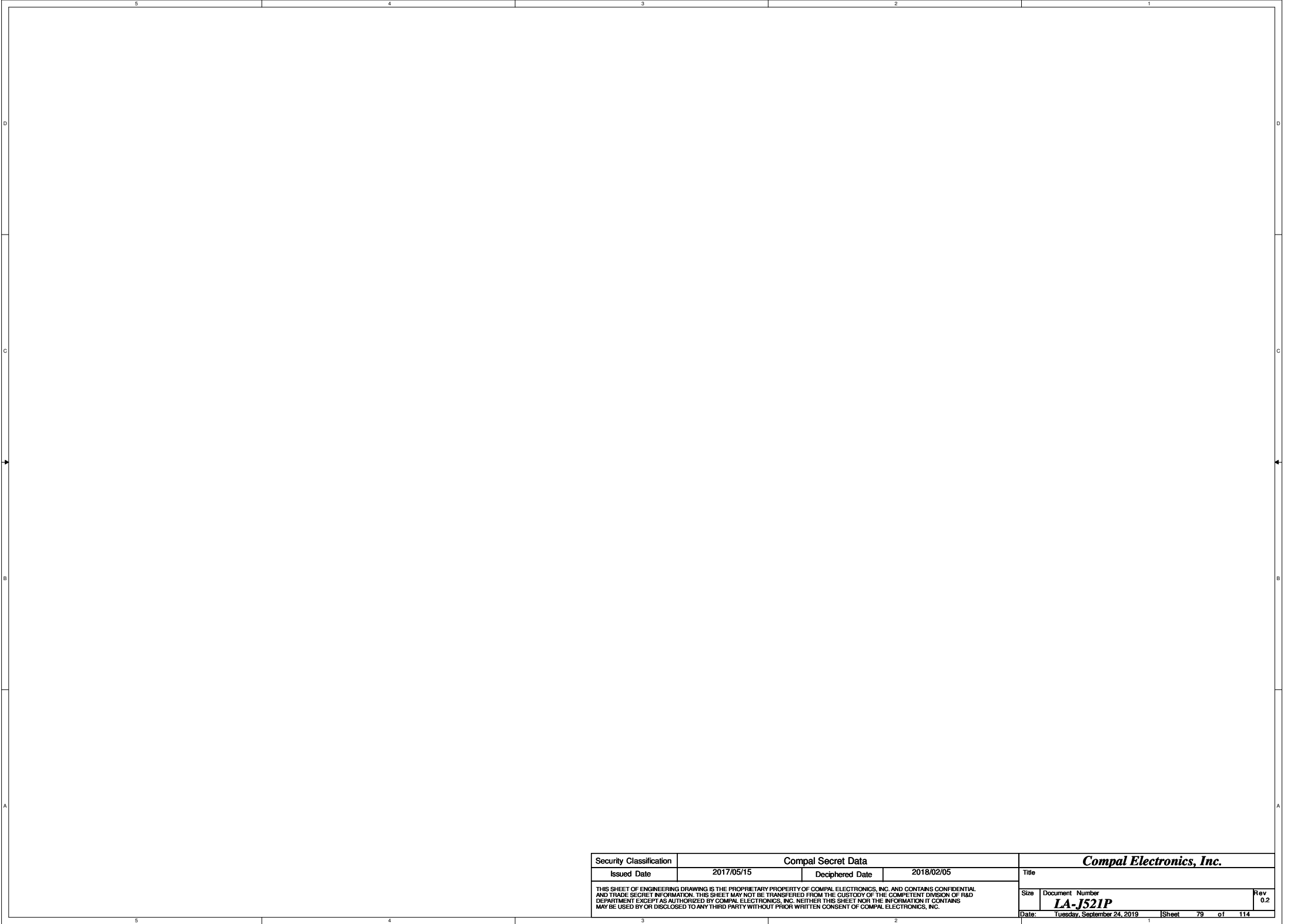


CPU FAN Control circuit



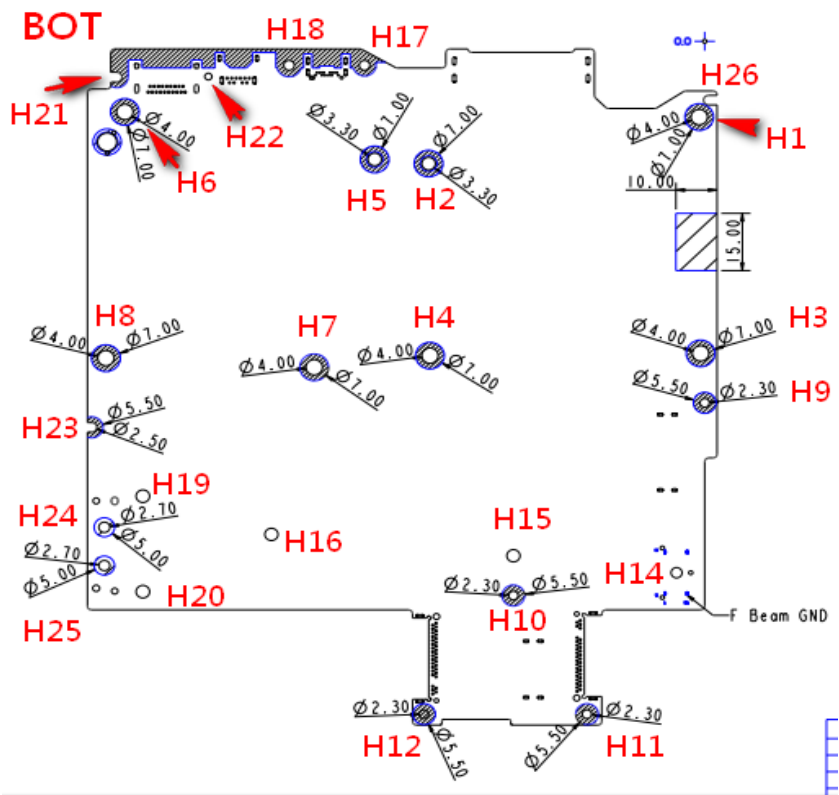
GPU FAN Control circuit

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Size	Document Number	Rev		0.2
Date:	Tuesday, September 24, 2019	Sheet	77	of 115

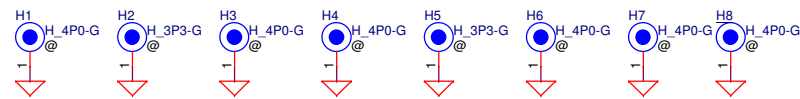


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Issued Date		2017/05/15		Deciphered Date		2018/02/05		Title							
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											<i>LA-J521P</i>			0.2	
								Date: Tuesday, September 24, 2019							
				Sheet		79		of 114							

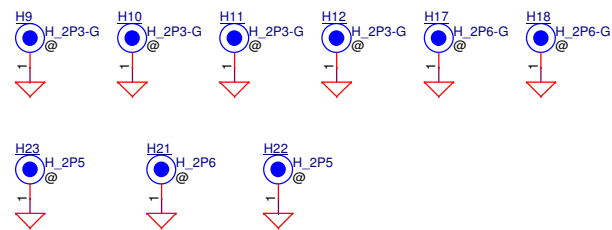
Main Func = Screw



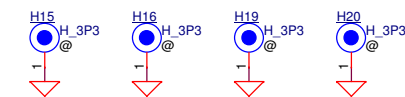
CPU & GPU



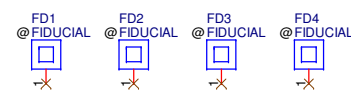
PTH



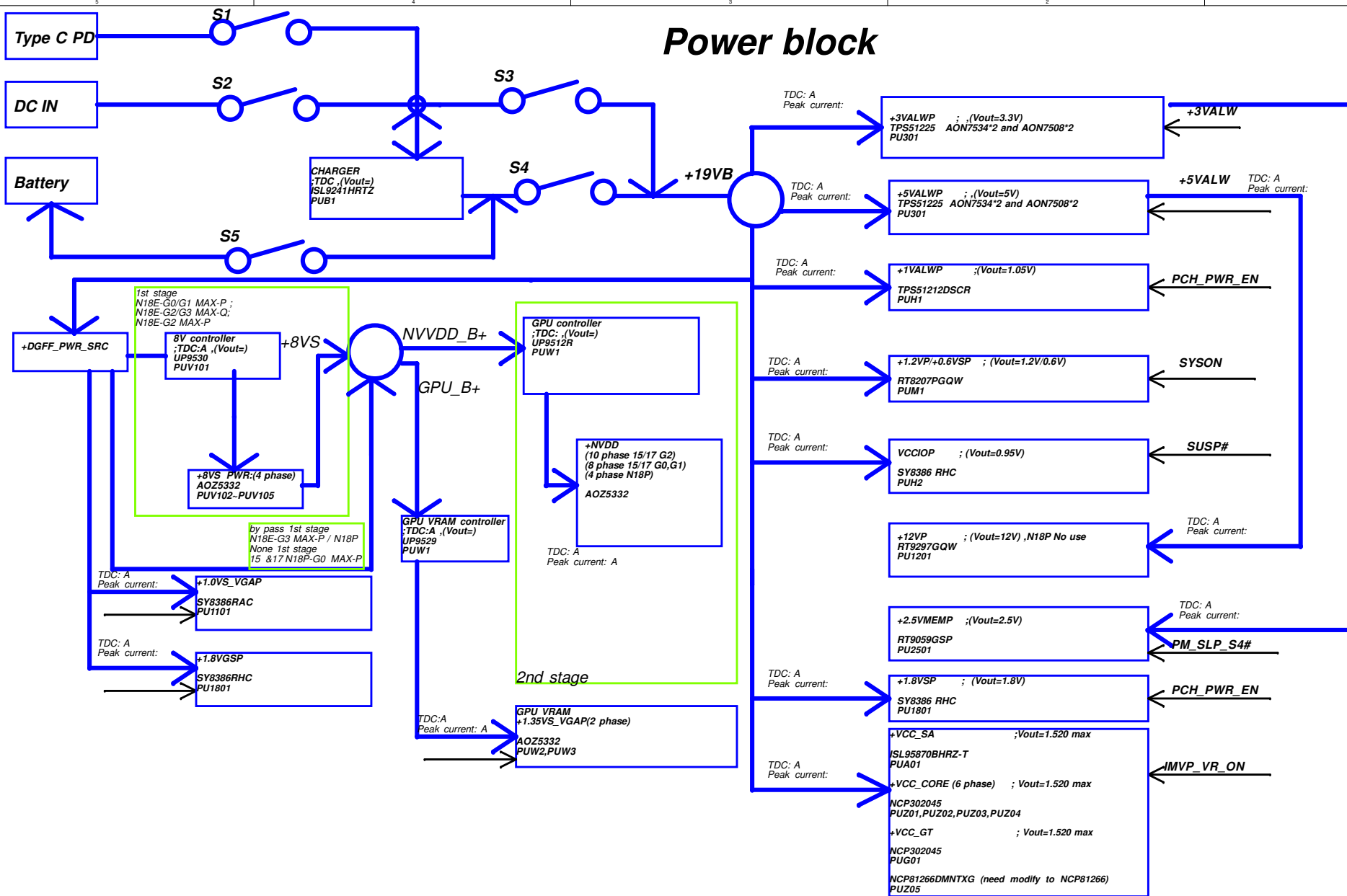
Stand-off



Fiducial Mark



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Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title	Screw Hole
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				Date:	Tuesday, September 24, 2019
				Sheet	80 of 115
				Rev	0.2

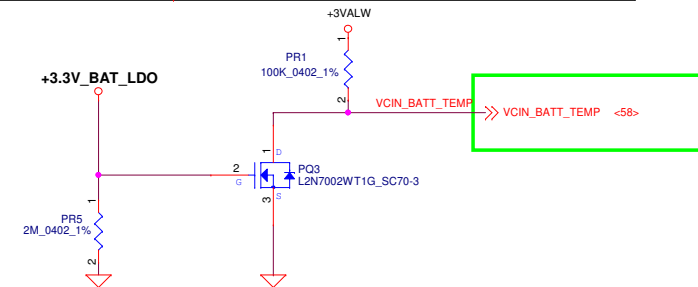
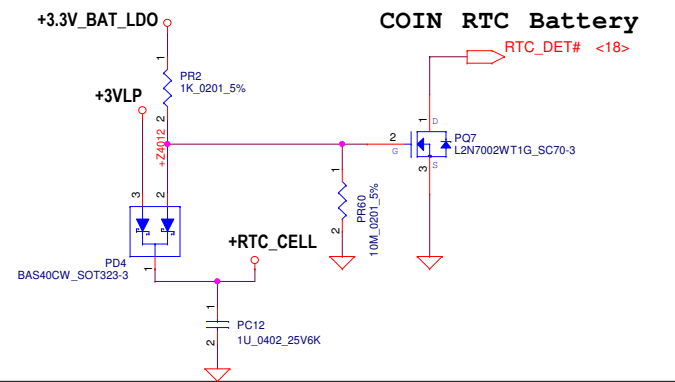
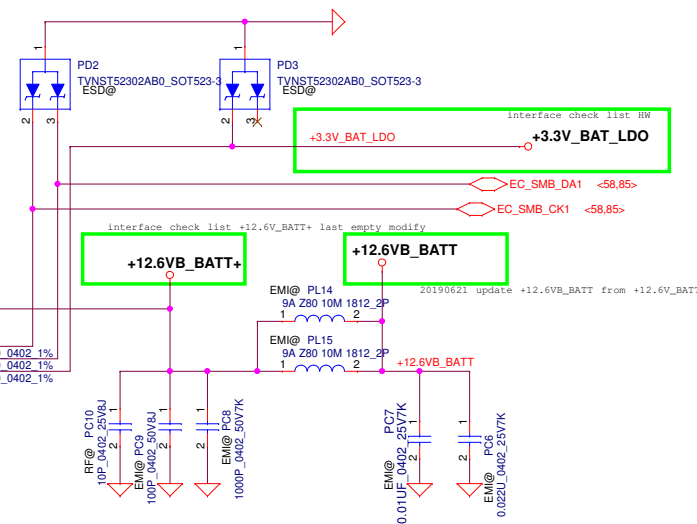
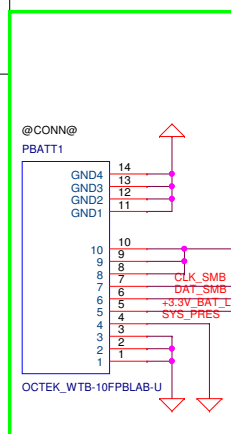


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				Size	Document Number	Rev
				LA-H191P		0.1
				Date:	Tuesday, September 24, 2019	Sheet 81 of 115

Battery 86W
86W/9V=9.56A

Battery connector:
1.GND
2.GND
3.GND
4.SYS_PRES
5.BATT_PRS
6.DAT_SMB
7.CLK_SMB
8.BATT++
9.BATT++
10.BATT++

confirm PJPBATT pin



battery unplug proshot

For PROCHOT

H_PROCHOT#

VCIN1_ADP_PROCHOT= 0.85V

reset = 0.81V

240W

VCIN1_ADP_PROCHOT=0.63V

reset = 0.59V

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

adapter unplug proshot

For PROCHOT

H_PROCHOT#

VCIN1_ADP_PROCHOT= 0.85V

reset = 0.81V

240W

VCIN1_ADP_PROCHOT=0.63V

reset = 0.59V

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

VCIN1_ADP_PROCHOT

CPU thermal protection

VCIN0_PH

Trig = 1V

93 +/- 3 degree C

Recover = 2.28V

50 +/- 3 degree C

VCIN0_PH

VCIN0_PH

VCIN0_PH

VCIN0_PH

VCIN0_PH

VCIN0_PH

VCIN0_PH

VCIN0_PH

VCIN0_PH

VCIN0_PH

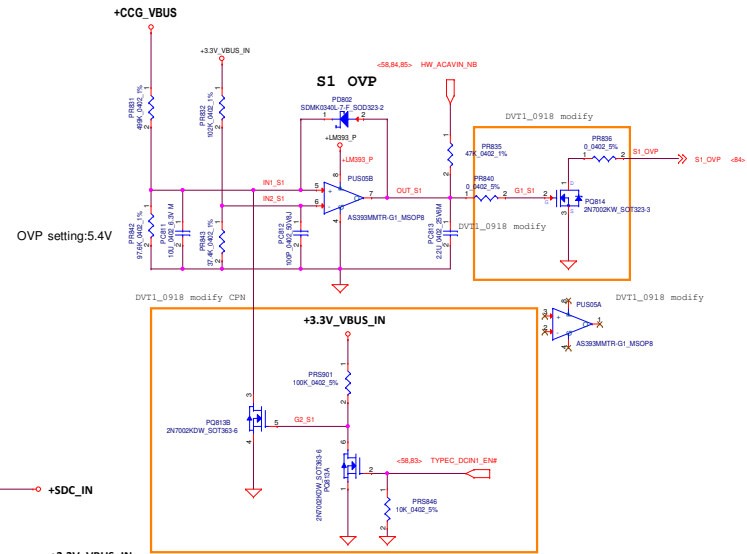
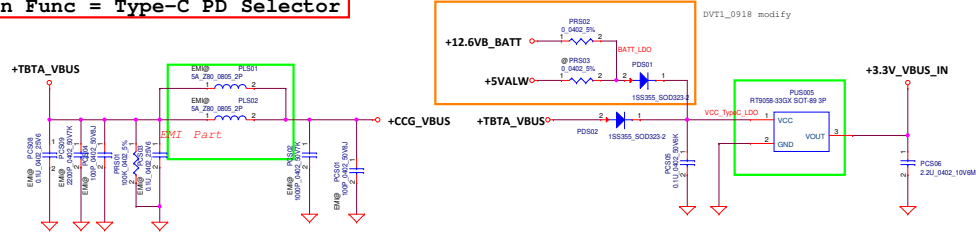
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VCIN0_PH

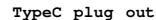
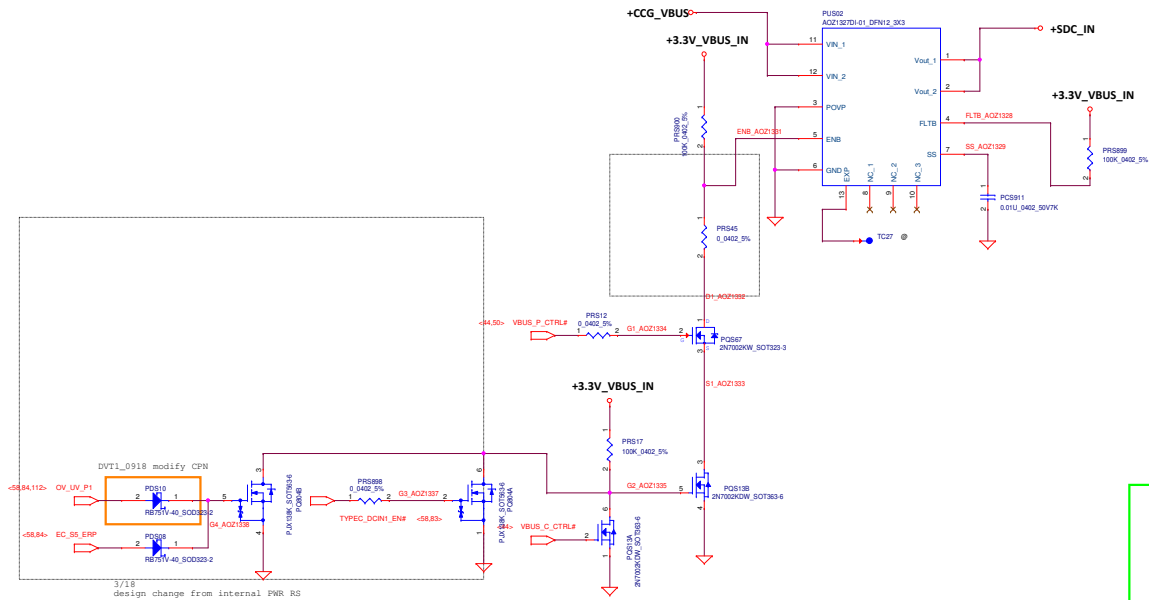
VCIN0_PH

VCIN0_PH

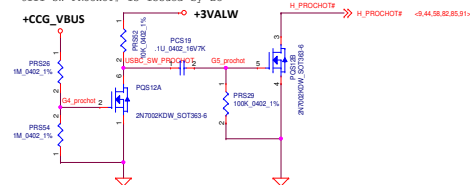
Main Func = Type-C PD Selector



Change to AOZ1327



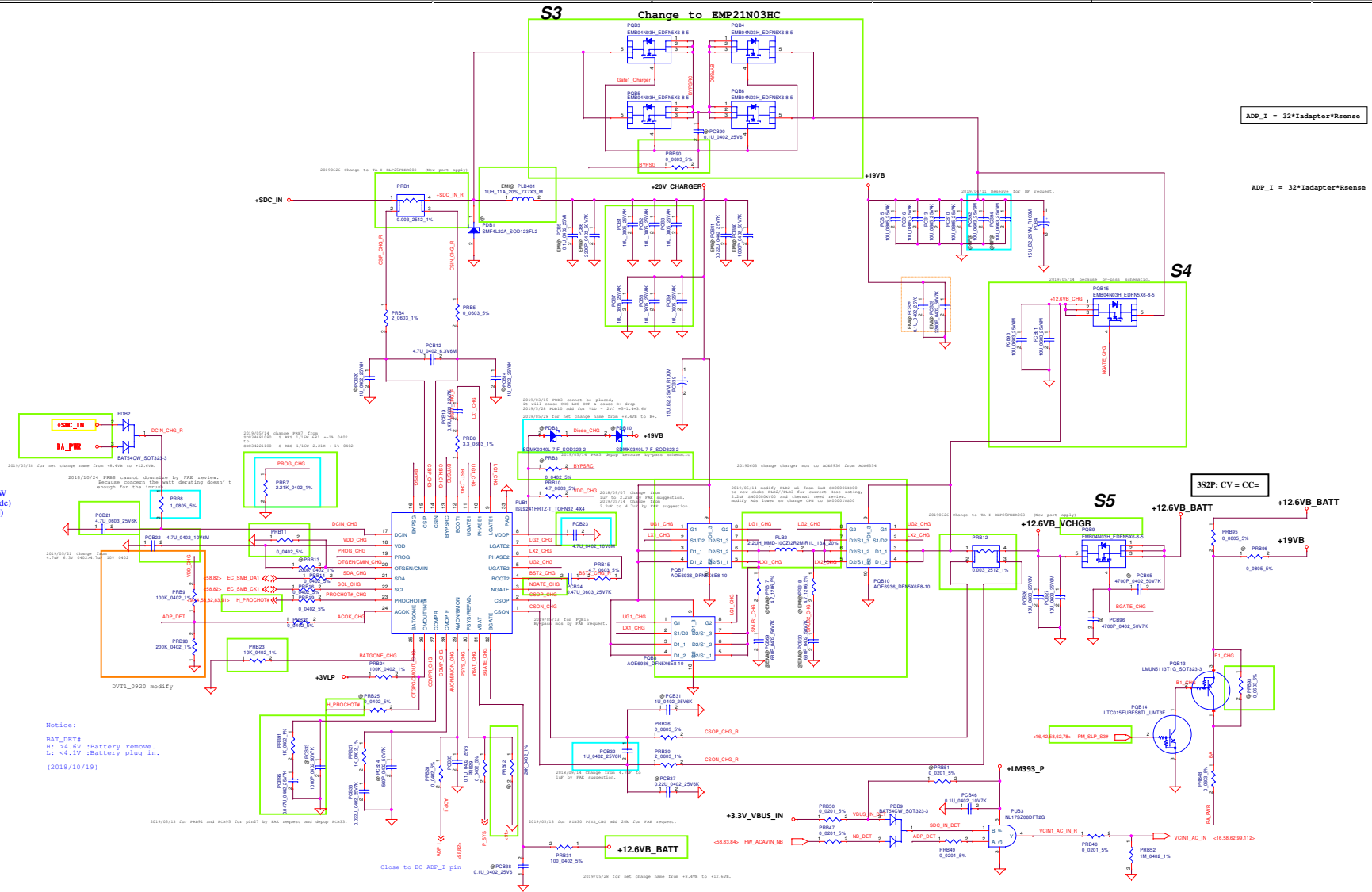
```
asserts H_PROCHOT# when TypeC is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC
```



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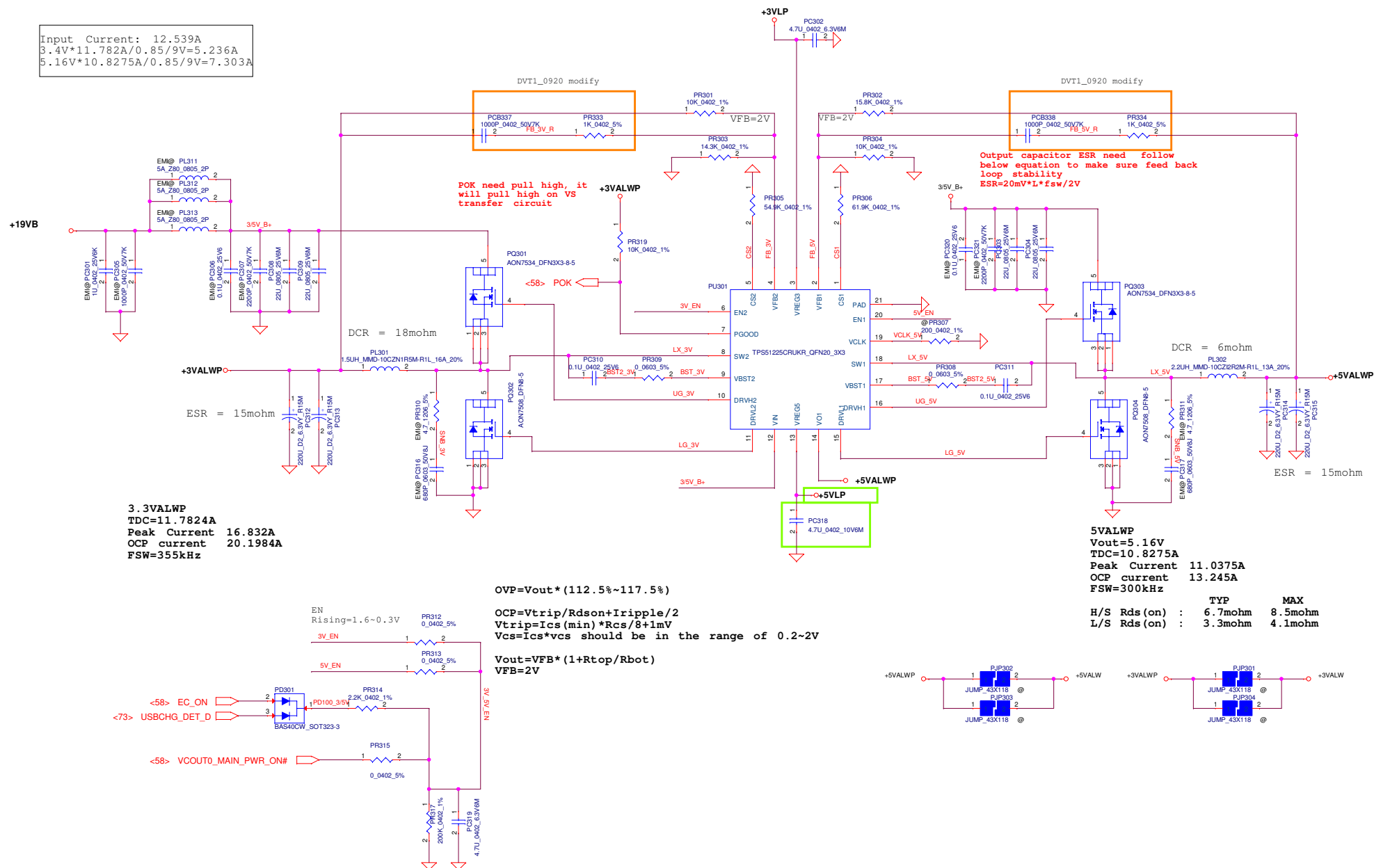
Battery information:
 3S1P (Cells)3S2P6cell
 12.6V/ 80Wh (nominal) : 12.6V/56W
 Charge Voltage: 13.2V (CC-CV Mode)
 Rated Charge Current: mA (normal)
 Fast charging : mA(1C/50%)
 Update by 2019/5/28

Notice:
 BAT_DET#
 H: +4.0V (Battery remove).
 L: +4.1V (Battery plug in).
 (2018/10/19)

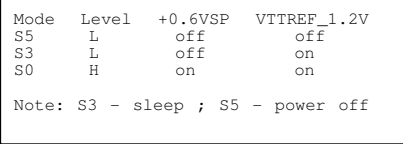


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				Drawn: Tzong-Hong Hsu	
				Check: Tzong-Hong Hsu	
				Date: Tuesday, September 24, 2019	

Input Current: 12.539A
 $3.4V \times 11.782A / 0.85 / 9V = 5.236A$
 $5.16V \times 10.8275A / 0.85 / 9V = 7.303A$

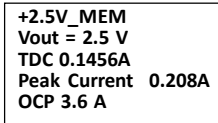


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title PWR +3.3VALWP+5VALWP		
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				Date:	Tuesday, September 24, 2019	Sheet 86 of 115

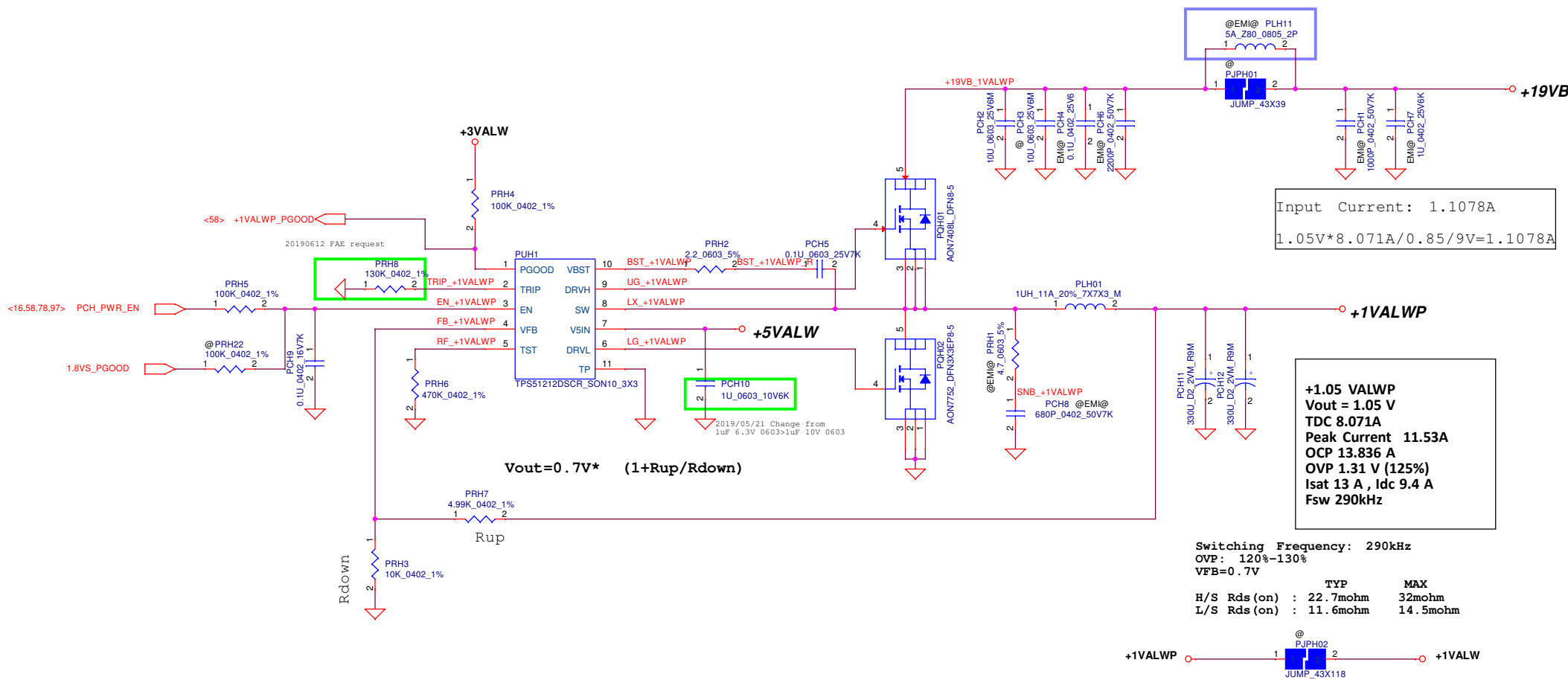
$$1.2V \cdot 6.68A / 0.85 / 9V = 1.047A$$


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				Size	Document Number	Rev.
				LAH551P		
Date: Tuesday, September 24, 2019				Sheet	87	of 115

Input	Peak	Current:0.208
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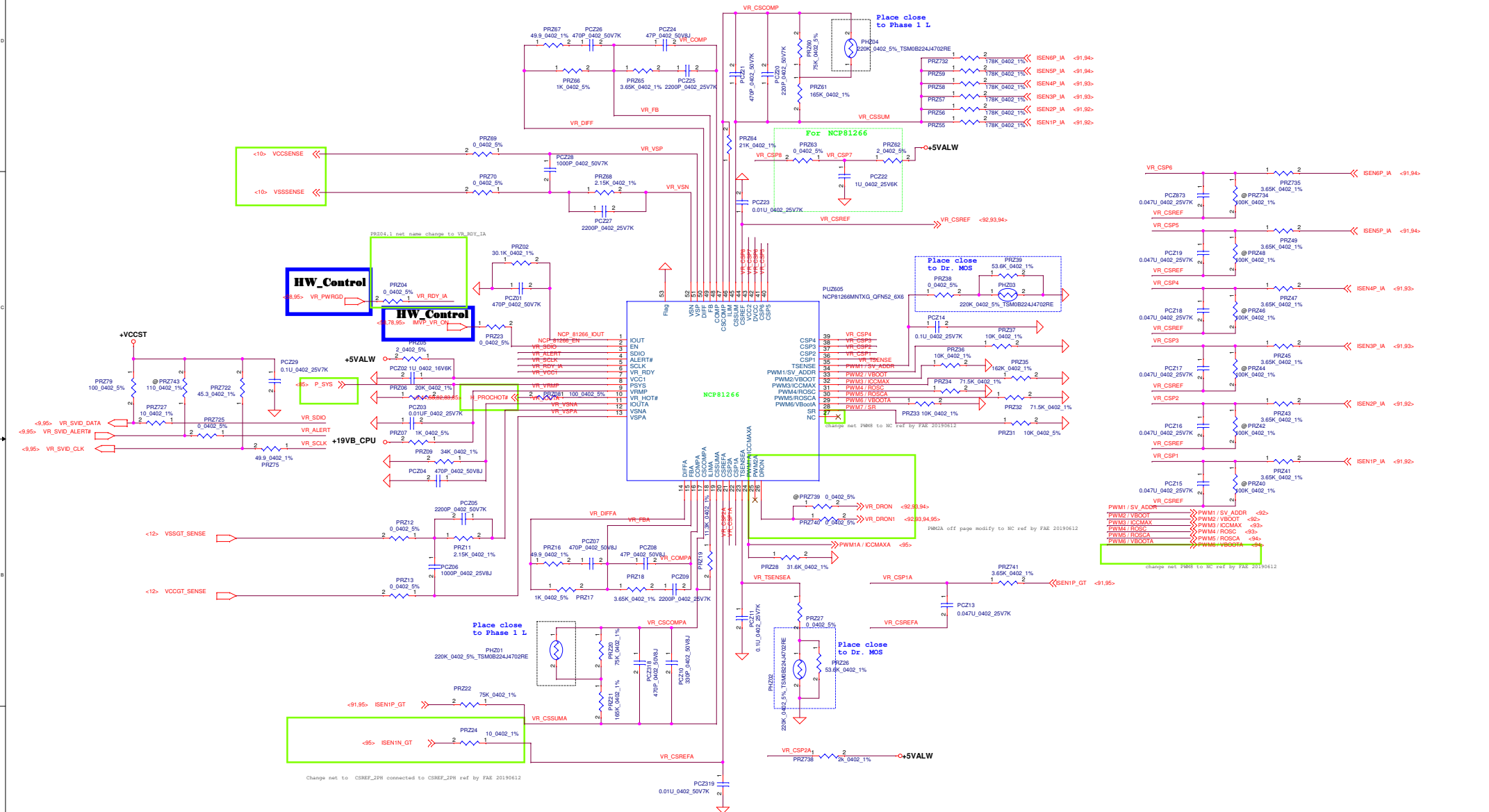
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Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title	PWR +1VALWP
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				LAH551P	
				Date	Tuesday, September 24, 2019
				Sheet	89 of 115
				Rev	0.1

Input Current: 0.7947A
 $0.95V \times 6.4A / 0.85 / 9V = 0.7947A$

+VCCIOP (0.95V)
TDC 4.48A
Peak Current 6.4 A
OCP Current 8A Fix by IC
TYP MAX
Choke DCR 24.0mohm , 27.0mohm



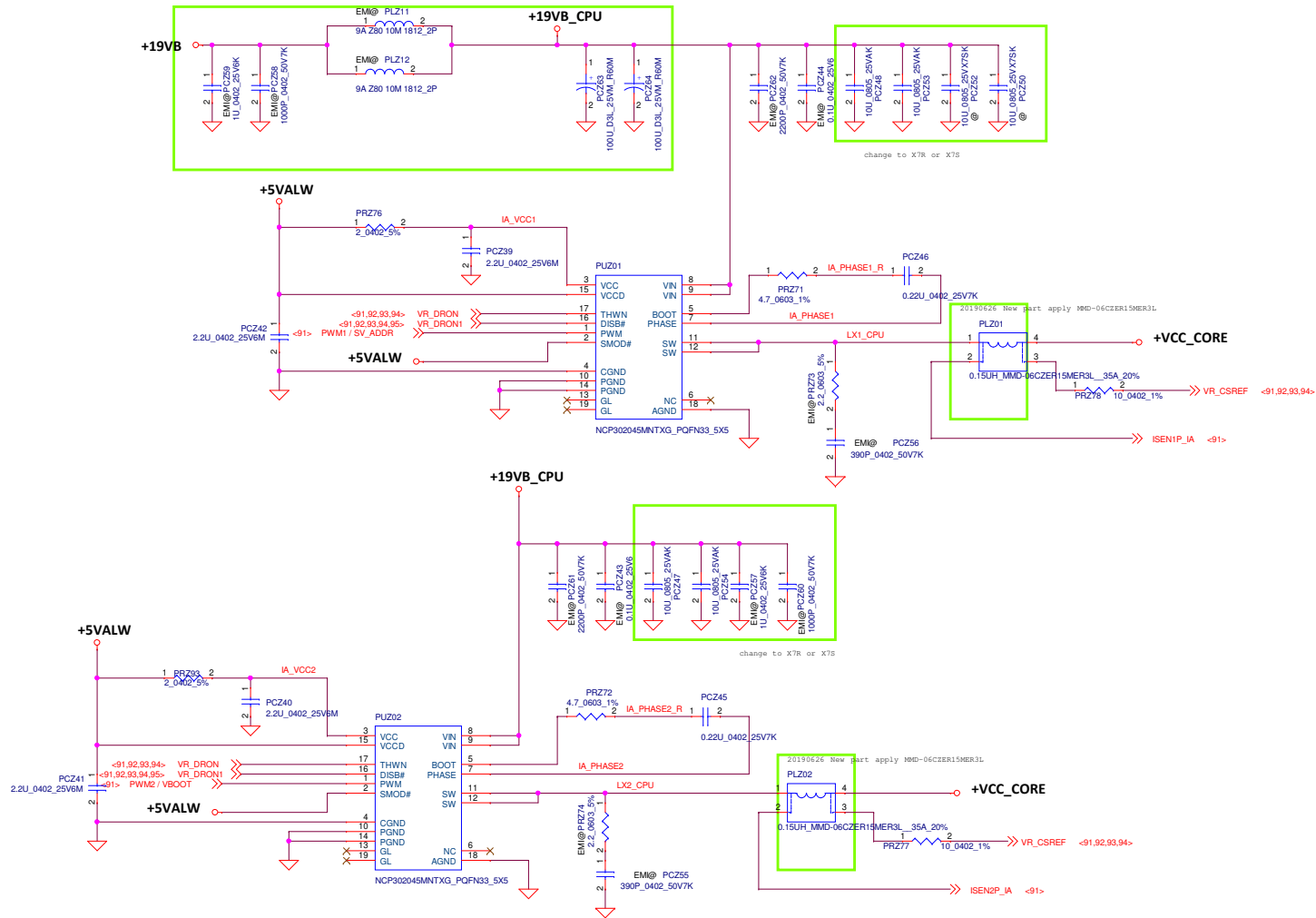
Security Classification	Compal Secret Data		
Issued Date	2018/05/16	Deciphered Date	2018/12/31
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D TO ANY OTHER DIVISION AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THE INFORMATION NOR THE INFORMATION CONTAINED HEREIN MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>			



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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	
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					91 of 115


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Main Func = CORE_Phase1&2
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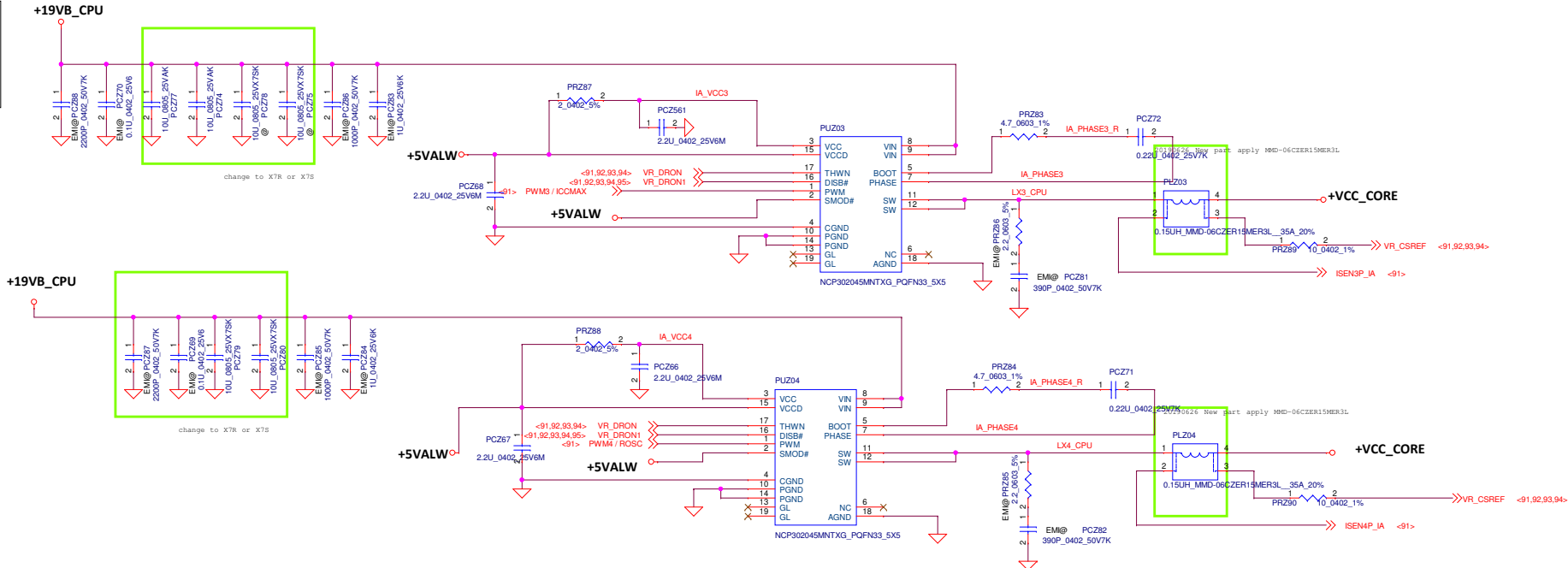
+VCC_CORE
TDC PL2 :146A
Peak Current 192A
OCP Current 230A
DCR mohm +/-5%



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title		
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				Size	Document Number	Rev
				LA-F611P 0.1		
Date: Tuesday, September 24, 2019				Sheet	92	of 115

Main Func = CORE_Phase3&4

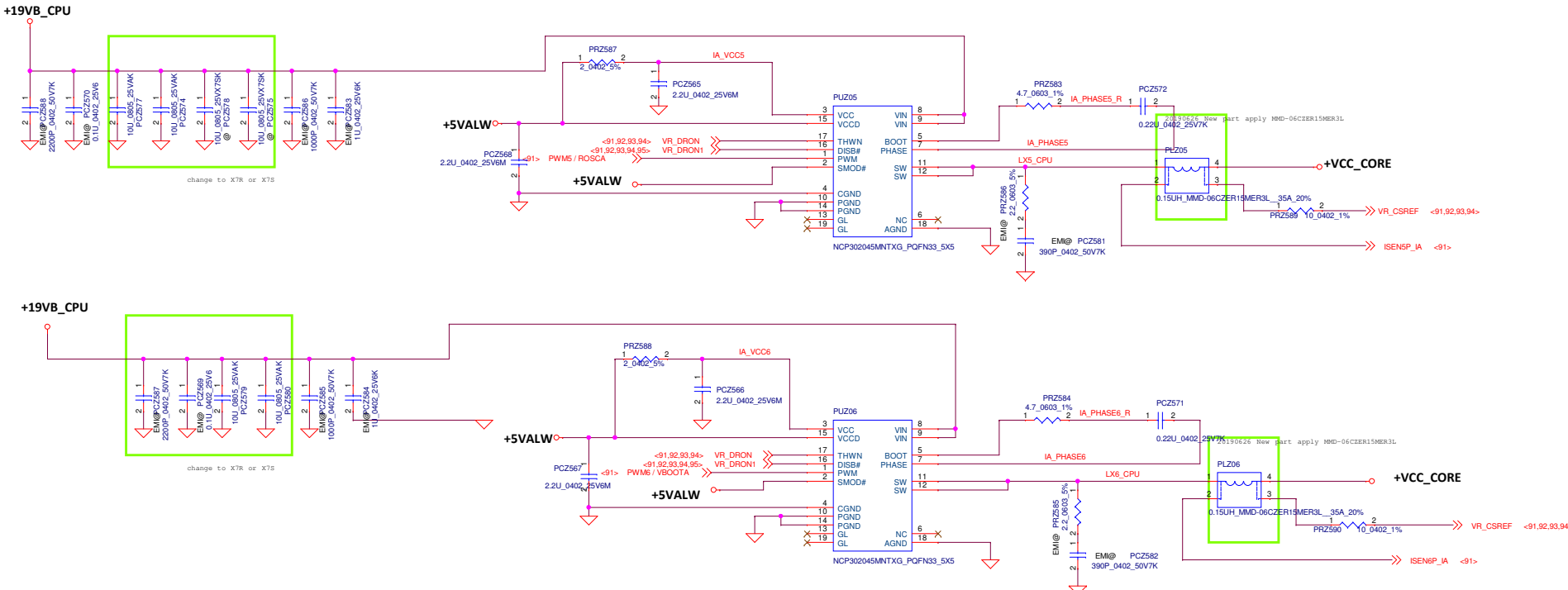
+VCC_CORE
TDC PL2 :146A
Peak Current 192A
OCP Current 230A
DCR mohm +/-5%



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	+VCC_CORE Phase3&4	
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				LA-F611P		0.1
Date: Tuesday, September 24, 2019				Sheet	93	of 115

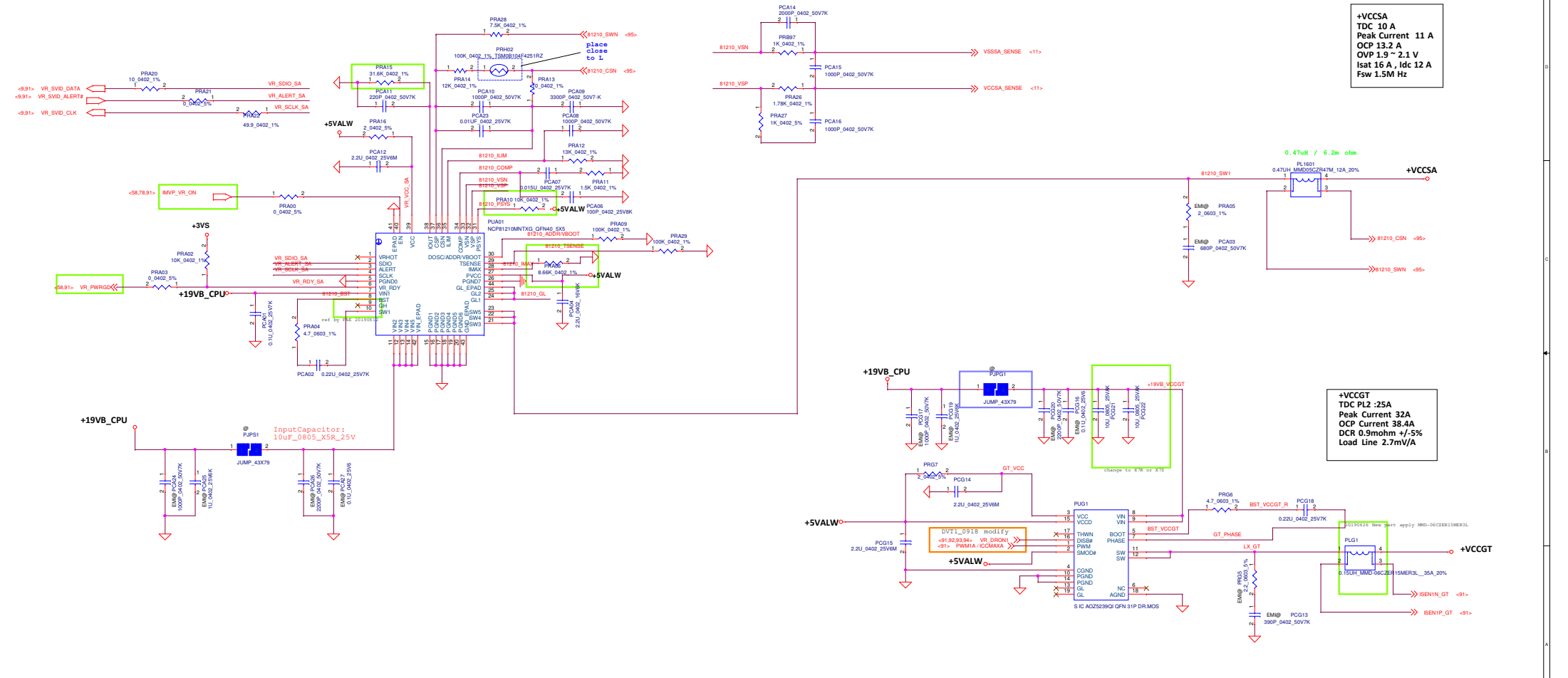
Main Func = CORE Phase3&4

+VCC_CORE
TDC PL2 :146A
Peak Current 192A
OCP Current 230A
DCR mohm +/-5%



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				Rev 0.1

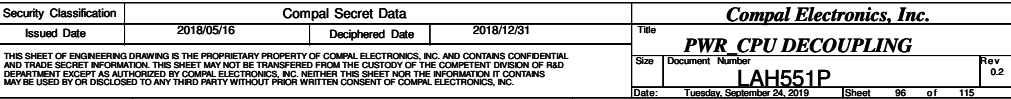
Main Func =+VCCSA

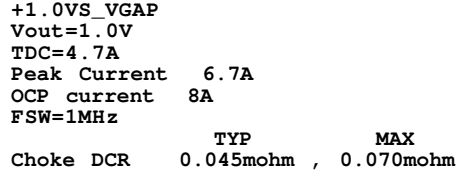


+VCCSA
TDC 10 A
Peak Current 11 A
OCP 13.2 A
OVP 1.9 ~ 2.1 V
Isat 16 A, Idc 12 A
Fsw 1.5M Hz

+VCCGT
TDC PL2 :25A
Peak Current 32A
OCP Current 38.4A
DCR 0.9mohm +/-5%
Load Line 2.7mV/A

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		PWR +VCC GT+VCC SA	
2016/01/06		2017/01/06		LA-FXXXX	
Size		Document Number		Rev	
Date		Tuesday, September 24, 2016		96	

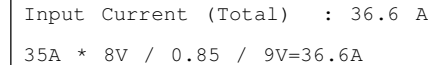




2019/05/14 because typec and barrel input
here change from PJPDC1 connector to B+

2019/05/14 because AMD no support CSSN and CSSP here change from current sense to Bead

Dr. MOS	phase	phase (4)
PRV419	10kohm	x
PRV411	x	0ohm
PRV403	0ohm	0ohm
PRV426	x	0ohm
PRV404	0ohm	x
PRV427	x	0ohm
PRV428	x	0ohm
PRV429	0ohm	x
PRV420	0ohm	0ohm
PRV421	x	0ohm
PRV422	0ohm	x
PRV423	x	0ohm
PRV424	x	0ohm
PRV425	0ohm	x
PRV119	2kohm	3.9kohm
PRV125	2kohm	3.9kohm
PRV131	2kohm	3.9kohm
PRV137	x	3.9kohm

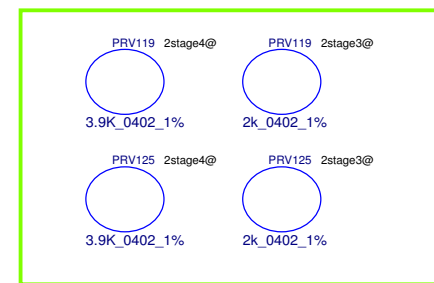
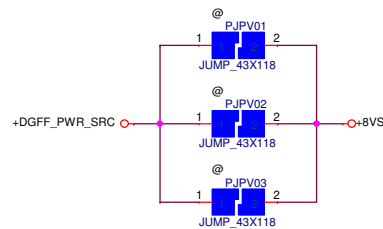


+8VS
TDC 35 A
Peak Current 50 A
OCP 80 A
Isat 50 A , Idc 35 A
Fsw 300k Hz

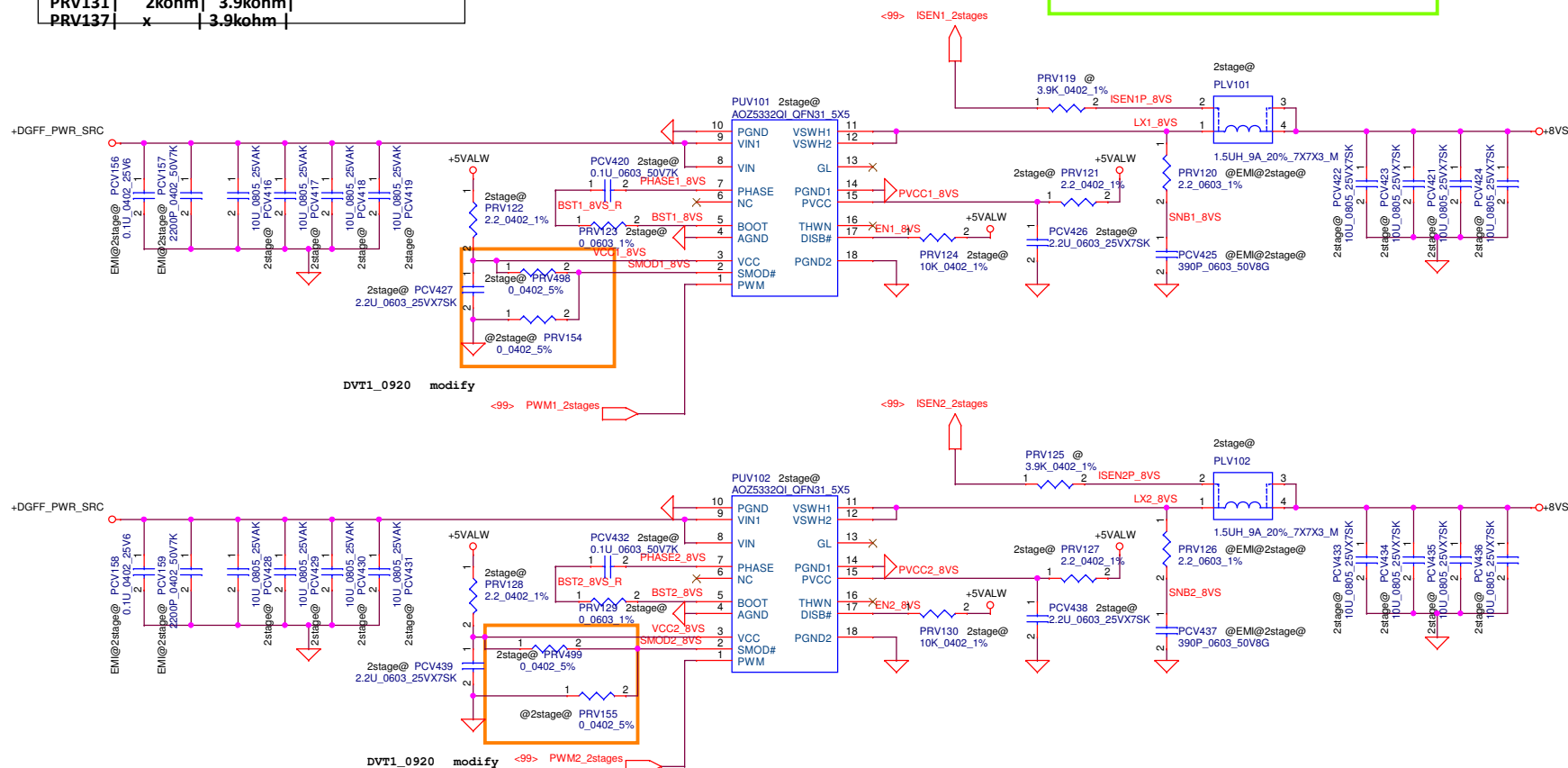
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2019/04/19	Deciphered Date	2020/04/19	Title	PWR_UP9530 Controller		
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				LS-J101P			0.1
				Date:	Tuesday, September 24, 2019	ISheet	99 of 115

$$35A * 8V / 0.85 / 9V = 36.6A$$

UP9530 3phase and 4phase BOM		
Dr.MOS)	3phase	4phase (2PWM to drive 4
PRV119	2kohm	3.9kohm
PRV125	2kohm	3.9kohm
PRV131	2kohm	3.9kohm
PRV137	x	3.9kohm



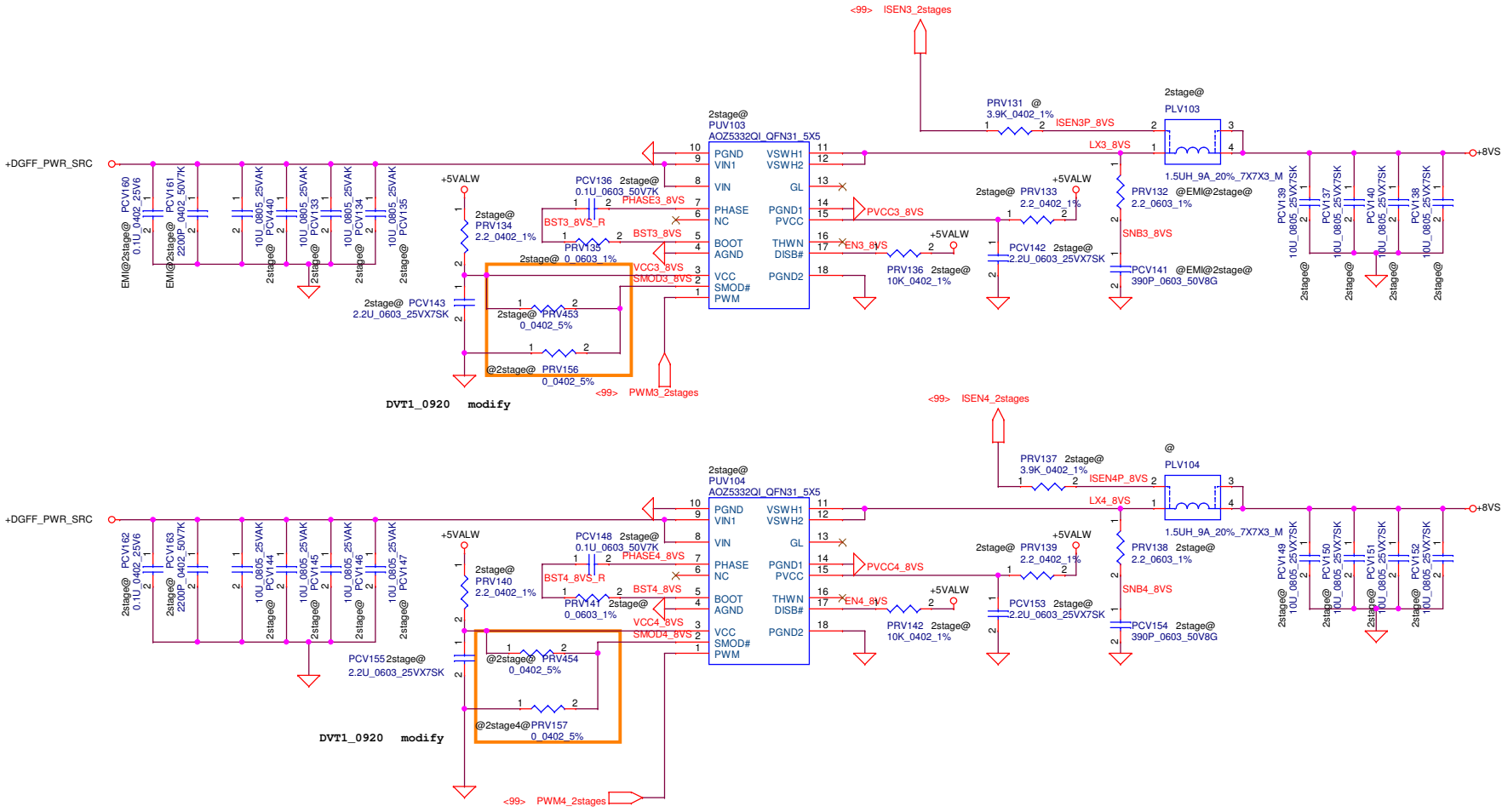
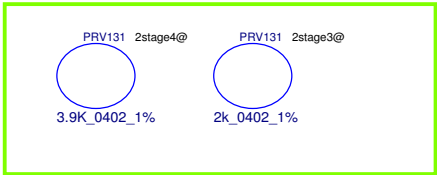
+8VS
TDC 35 A
Peak Current 50 A
OCP 80 A
Isat 50 A , Idc 35 A
Fsw 300k Hz



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Issued Date	2019/04/19	Deciphered Date	2020/04/19	Title		
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				Size	Document Number	Rev
				LS-J101P		0.1
				Date:	Tuesday, September 24, 2019	Sheet 100 of 115

Input Current (Total) : 36.6 A
35A * 8V / 0.85 / 9V=36.6A

+8VS
TDC 35 A
Peak Current 50 A
OCP 80 A
Isat 50 A , Idc 35 A
Fsw 300k Hz



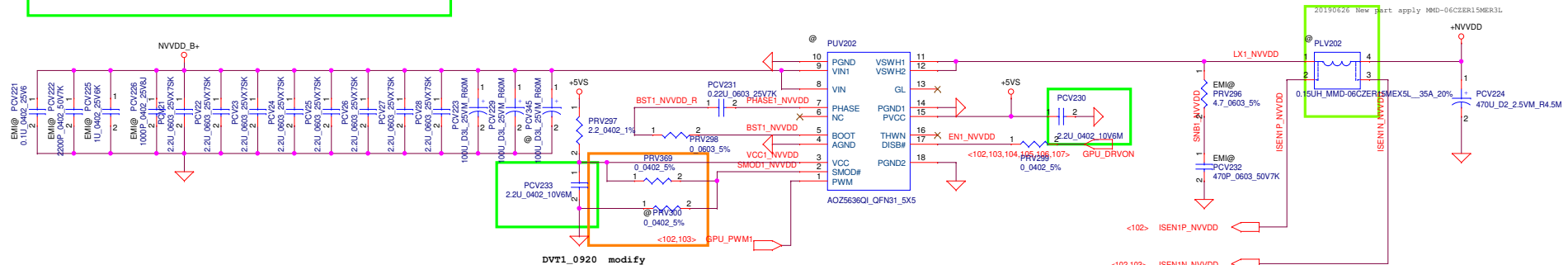
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Issued Date	2019/04/19	Deciphered Date	2020/04/19	Title	
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Size	Document	Number		Rev	
				LS-J101P	
Date:	Tuesday, September 24, 2019	Sheet	101	of 115	



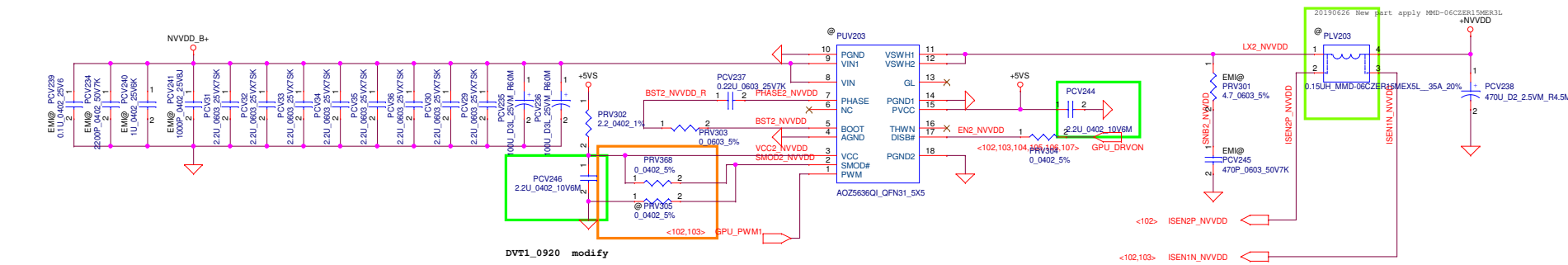
+NVVDD (N18E - G3)
TDC 144A
Peak Current 450 A
OCP 540 A
OVP 1.43 V
Isat 50 A, Idc 25 A
Fsw 300K Hz

Input Current (Total) : 25.1 A
 $180A \times 0.95V / 0.85 / 8V = 25.1A$

2019/07/10 Add Choke BOM



DVT1_0920 modify



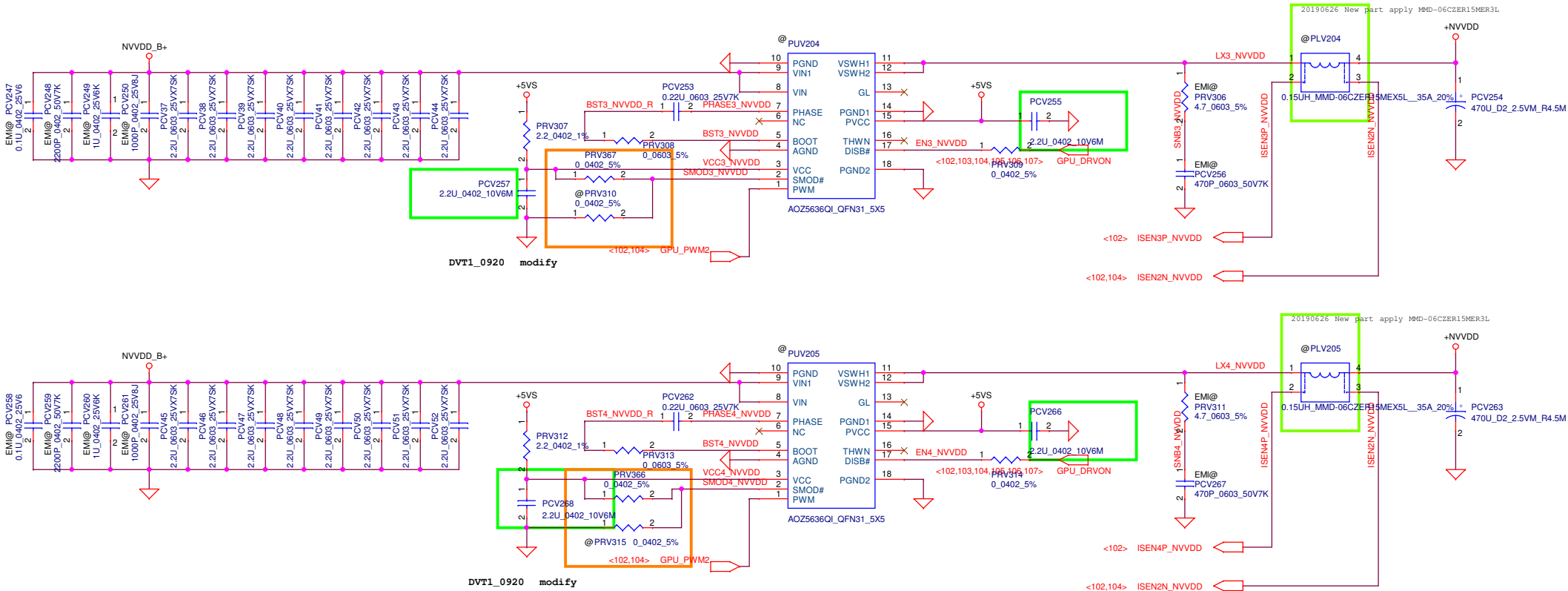
DVT1_0920 modify

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				Date	LS-1101P
				Sheet	103 of 115

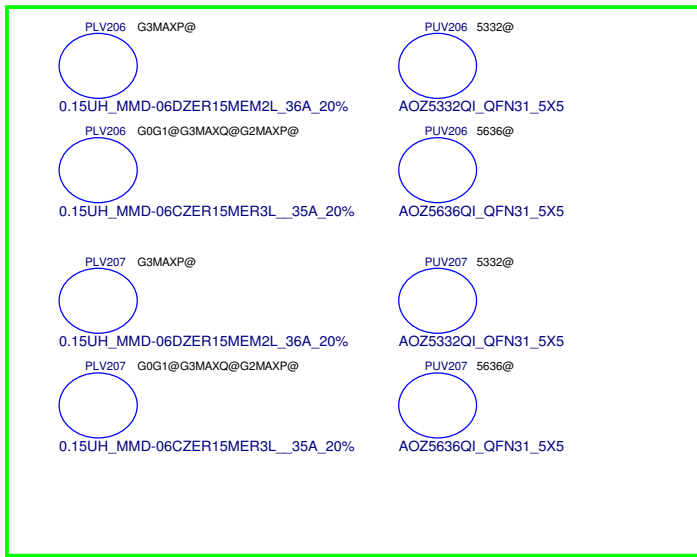


+NVVDD (N18E - G3)
TDC 180 A
Peak Current 450 A
OCP 540 A
OVP 1.43 V
Isat 50 A , Idc 25 A
Fsw 300k Hz

Input Current (Total) : 25.1 A
 $180A \times 0.95V / 0.85 / 8V = 25.1A$

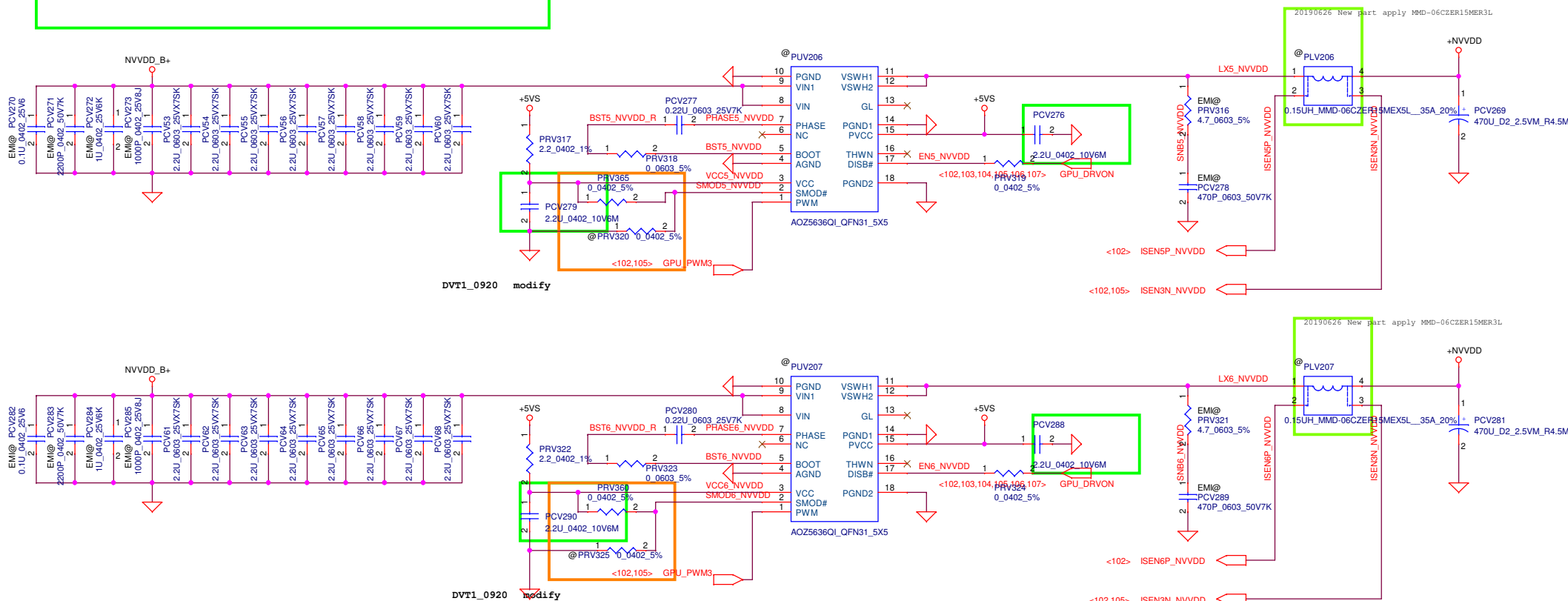


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Issued Date	2019/04/19	Deciphered Date	2020/04/19	Title	
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Size	Document	Number		Rev	0.1
Date: Tuesday, September 24, 2019				Sheet	104 of 115



+NVVDD (N18E - G3)
TDC 180 A
Peak Current 450 A
OCV 540 A
OVP 1.43 V
Isat 50 A, Idc 25 A
Fsw 300k Hz

Input Current (Total) : 25.1 A
 $180A \times 0.95V / 0.85 / 8V = 25.1A$

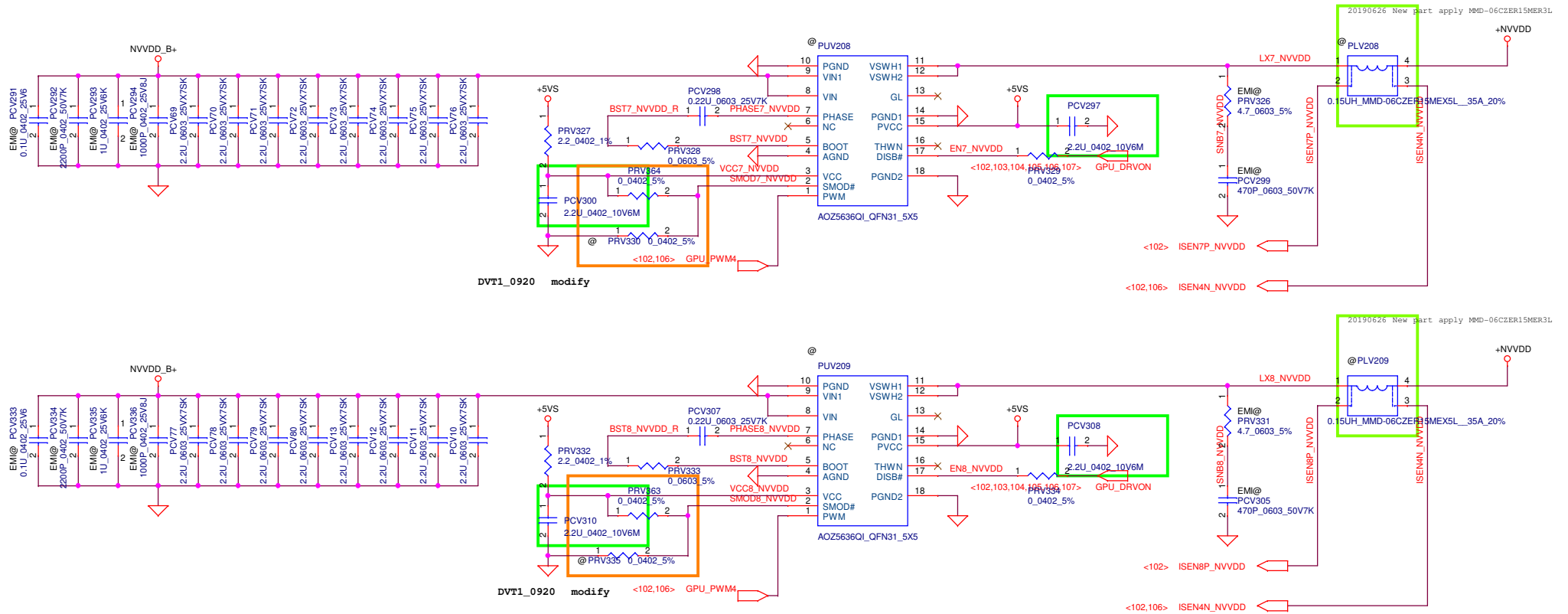


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								Document Number	
								LS-J101P	
								Rev 0:	
		Date:		Tuesday, September 24, 2019		Sheet		105 of 115	



+NVVDD (N18E - G3)
TDC 180 A
Peak Current 450 A
OCP 540 A
OVP 1.43 V
Isat 50 A, Ildc 25 A
Fsw 300k Hz

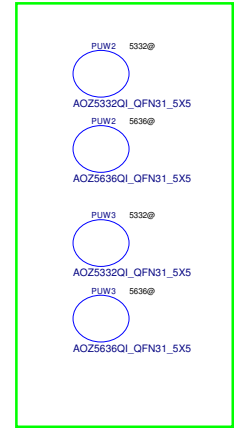
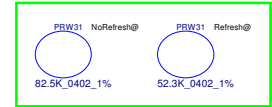
Input Current (Total) : 25.1 A
 $180A \times 0.95V / 0.85 / 8V = 25.1A$



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2019/04/19		Deciphered Date		2020/04/19		Title	
										PWR +NVVDD Phase7&8	
										Size Document Number	
										LS-J101P	
										Date: Tuesday, September 24, 2019	
										Sheet 106 of 115	
										Rev 0.1	

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Nvidia Refresh BOM Table									
GPU	C1	C2	C3	C4	C5	C6	C7	C8	C9
1.35V	V	V	V	V	V	V	V	V	V
1.25V	V	V	V	V	V	V	V	V	V
1.2V	V	V	V	V	V	V	V	V	V



BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW30	PRW31
	N18E G2/G3		SAMSGUNG/MICRON	1.35V	21K	@

Security Classification	Compal Secret Data		Deciphered Date		Title	
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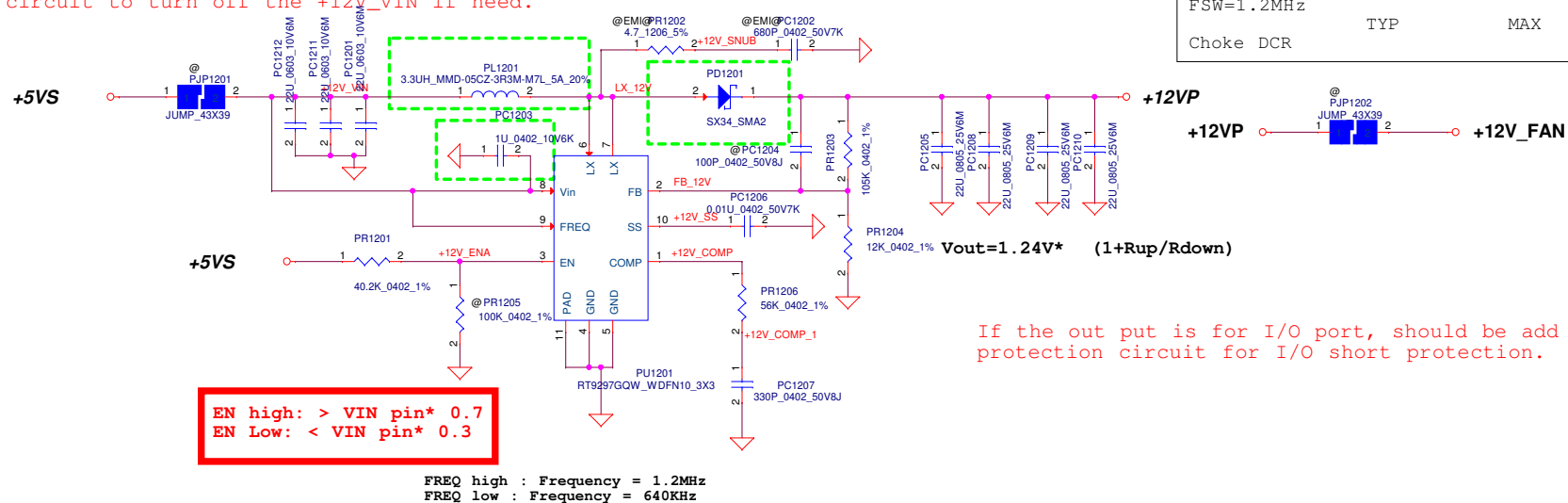
A

Input Current: 2.26A
 $12V \times 0.8A / 0.85 / 5V = 2.26A$

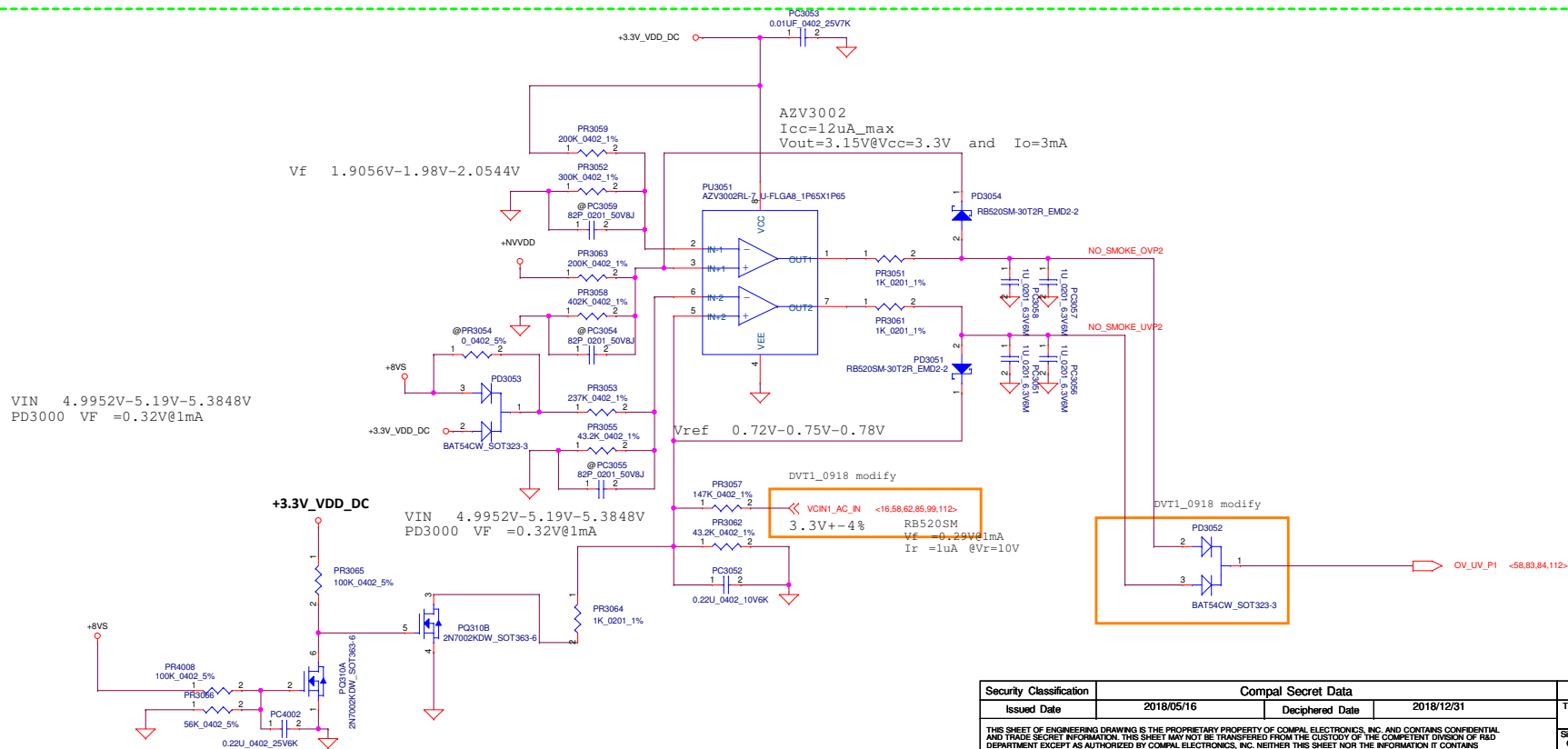
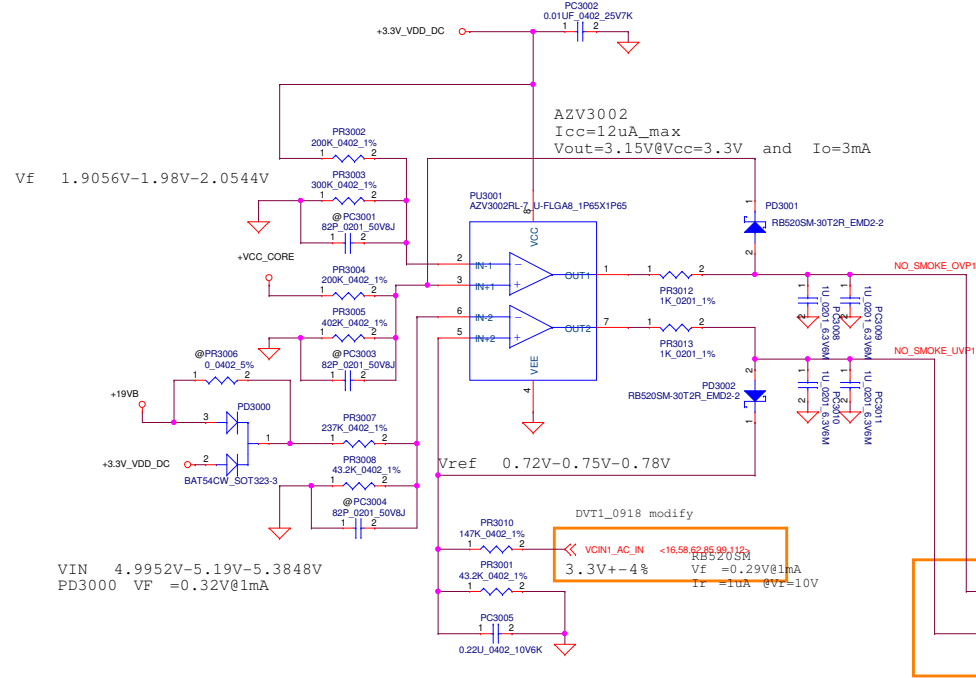
+12VP
 TDC 0.56A
 Peak Current 0.8A
 OCP current 3A
 FSW=1.2MHz
 Choke DCR TYP MAX

Add a switch circuit to turn off the +12V_VIN if need.

Must check PL1201 and PD1201 rating for your application.



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